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Editorial

Fast communication is the need of the hour for which society relies on Electronics &Telecommunication Engineering for breakthroughs in applications such as satellites, next generation mobile phones, air-traffic control, the Internet etc.

In fact, all electronic devices need software interface to run and come with one other or other device controlling programs architected and developed by electronics and communication Engineering. Thus, tremendous opportunities for research and development lies in the area of Electronics and Communication Engineering, as everyday consumer need new devices to support them in daily life.

International Conference on Electronics and Communication Engineering (ECE-2012) provides such unique platform for R&D works. The conference will conglomerate academicians, researchers from all types of institutions and organizations who would share their domain knowledge and healthy interaction would take place covering the areas like electronics and communications engineering, electric energy, automation, control and instrumentation, computer and information technology, and the electrical engineering aspects of building services and aerospace engineering, The wide scope encompasses analogue and digital circuit design, microwave circuits and systems, optoelectronic circuits, photo voltaic, semiconductor devices, sensor technology, transport in electronic materials, VLSI technology and device processing.

I must acknowledge your response to this conference. I ought to convey that this conference is only a little step towards knowledge and innovation but certainly in the right perspective. I wish all success to the paper presenters I extend heart full thanks to members of faculty from different institutions, research scholars, delegates, IRNet Family members, members of the technical and organizing committee. Above all I note the salutation towards the almighty.

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Low Power 2:1 Multiplexer Design Using DCVS Logic and Its Application in 1-Bit Full Adder Cell

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Abstract **-** This paper is based on prelayout simulations of a proposed design of 2:1 multiplexer circuit that shows improved performance than the existing 2:1 multiplexer circuit and its application in 1 bit full adder cell. The proposed design demonstrates the superiority in terms of power–delay product, temperature sustainability and frequency when compared with existing 2:1 multiplexer. All simulations are performed on 45nm standard model on Tanner EDA tool version 13.0.

Keywords **-** *CMOS Logic, 2:1 multiplexer Low power, 1 bit full adder, and VLSI.*

I. INTRODUCTION

Low power design of VLSI circuits has been identified as a critical technological need in recent years due to high demand for portable consumer electronic products. With the explosive growth in laptops, portable personal communications systems and the evolution of the shrinking technology, the research effort in low-power microelectronics has been intensified and low power VLSI system have emerged high man hind. A 2:1 multiplexer is a basic building block of the "switch logic". In many computers and other kinds of processors, adders are used not only in the arithmetic logic units, but also in other parts of the processor, where they are used to calculate addresses. It is also an important element in many variant circuit designs, such as the implementation of an FPGA and memory circuits. Multiplexer and adders have a direct impact on power consumption and speed of VLSI systems. Therefore study on multiplexer and adder is inevitable [1].

II. PRIOR WORK

In this paper, we explore the Differential Cascode Voltage-Switch Logic (DCVSL) circuit design methodology. The key benefits of DCVSL are consumes no static power (like standard CMOS), uses latch to compute output quickly, requires true/complement inputs, produces true/complement outputs. Allows "Complex" gates, never needs inverters in the logic path and low power consumption [2], [3]. A logic function and its inverse are automatically implemented in this logic style [4], [5]. The schematic diagram of existing DCVSL 2:1multiplexer is shown in figure1. The pull-down network implemented by the NMOS logic tree generates complementary output. This logic family is also known as Differential Cascode Voltage Switch Logic (DCVS or DCVSL).The advantage of DCVSL is in its logic density that is achieved by elimination of large PFETS from each logic function [6]-[8]. It can be divided it to two basic parts: a differential latching circuit and a cascoded complementary logic array.

S	A	B	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Table I : Truth table of 2:1 multiplexer

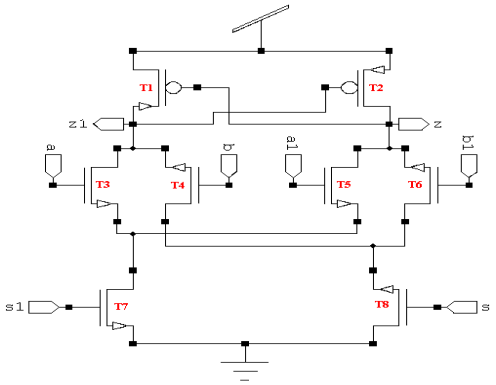

Fig. 1 : Schematic of existing 2:1 multiplexer

III. PROPOSED 2:1 MULTIPLEXER DESIGN

By adding two NMOS transistors T1 and T4 in the pull up part of existing 2:1 multiplexer the circuit shows a remarkable improvement over the existing design. In the proposed circuit due to the excess added transistors there is a reduction in threshold loss for the circuit, which further causes the reduction in overall power consumption of the circuit. Due to the transmission gate topology in the proposed design the circuit shows better output waveforms in terms of threshold loss as shown in figure 6. The two logic trees are capable of processing complex functions within a single circuit delay. The schematic of proposed 2:1multiplexer is shown in figure2.

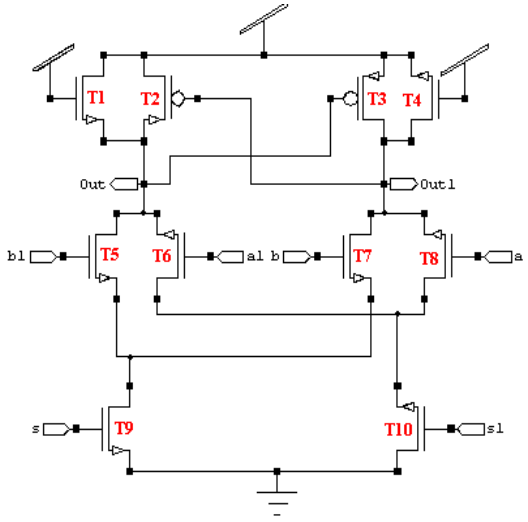

Fig. 2 : Schematic of proposed 2:1 multiplexer

IV. SIMULATION AND COMPARISON

All schematic simulations are performed on Tanner EDA tool version 13.0 using 45nm technology with input voltage ranges from 0.6V to 1.4 V. In order to prove that proposed design is consuming low power and has better performance, simulations are carried out for power, delay, power-delay product at varying supply voltages, temperatures and operating frequencies. To establish an impartial testing environment both circuit have been tested on the same input patterns which covers all combinations of the input stream. The graph shown in figure3 reveals that the power consumption of proposed 2:1 multiplexer is remarkably reduced than the existing 2:1 multiplexer at 45nm technology. Proposed 2:1 multiplexer shows slightly less delay than the delay of existing 2:1 multiplexer for input voltage ranging from 0.6V to 1.4V which shown in figure4. Similar results for power consumption vs. frequency and power consumption vs. temperature are shown in figure5 and figure6 respectively at 45nm technology. Table II show the power delay product over a range of power supply voltages and as it is shown in the table that proposed 2:1 multiplexer circuit show minimum power delay product.

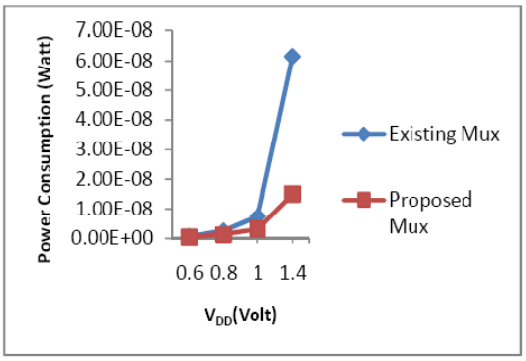

Fig. 3 : Power consumption comparison of existing and proposed multiplexer at different supply voltages

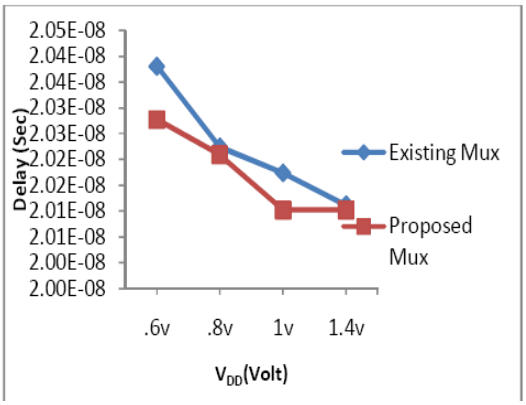

Fig. 4 : Delay comparison of existing and proposed multiplexer at different supply voltages

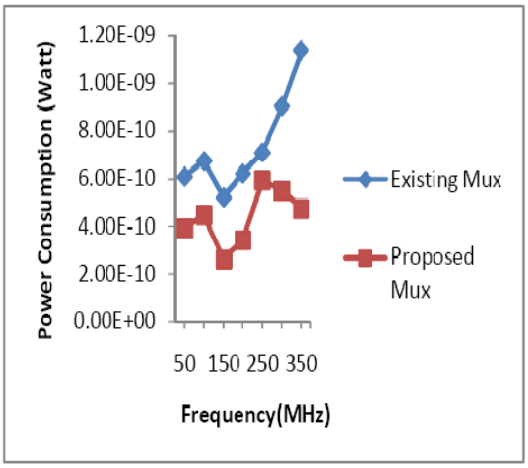

Fig. 5 : Power Consumption comparison of existing and proposed multiplexer at different frequencies

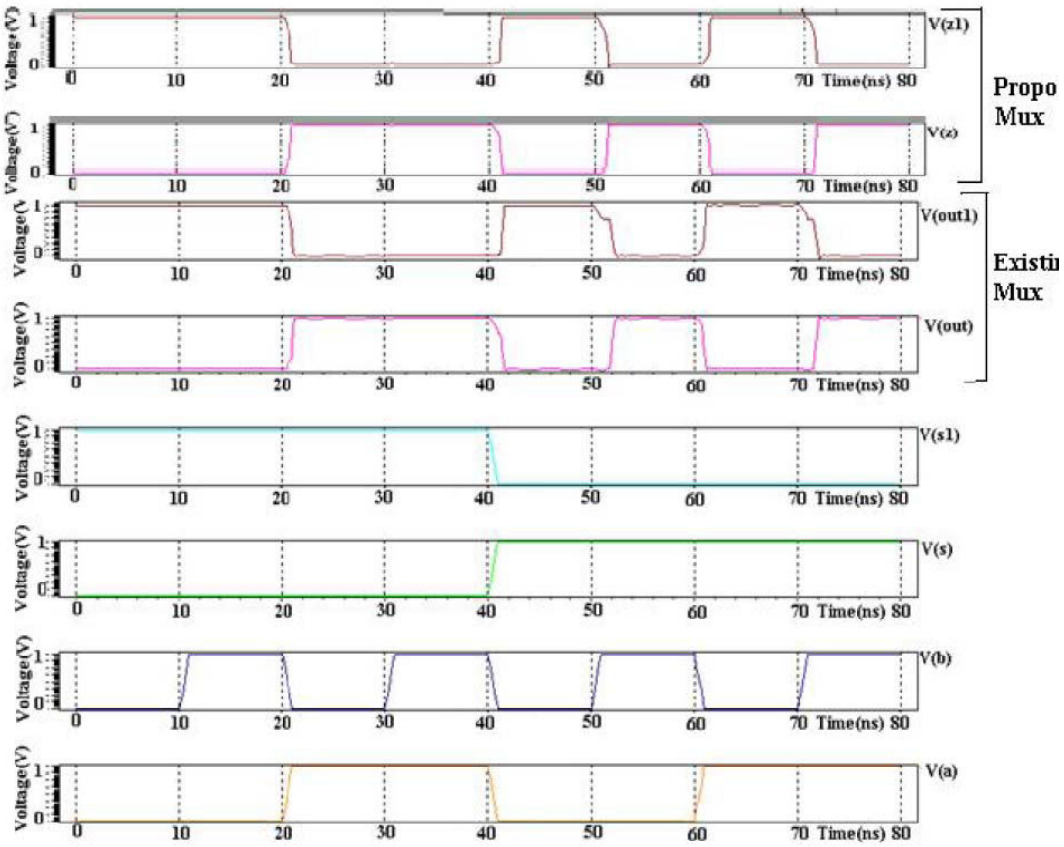

Fig. 6 : In-Out waveforms of Existing 2:1 multiplexer and proposed 2:1 multiplexer

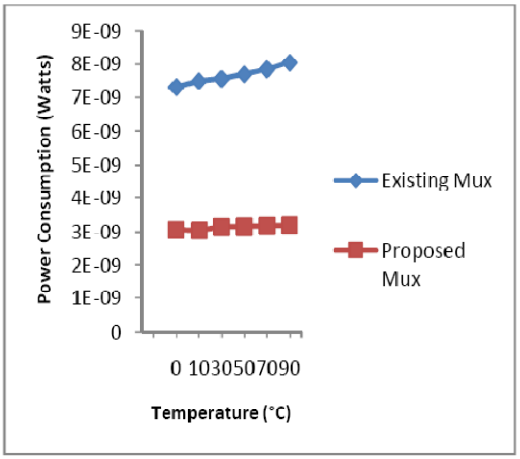

Fig. 7 : Power consumption comparison of existing and proposed multiplexer at different temperature

V_{DD} (volts)	Power Delay Product(Watt-sec) (45nm)	
	Existing Mux	Proposed Mux
.6	1.24106E-17	7.99194E-18
.8	5.09886E-17	2.59553E-17
1	1.51653E-16	6.34903E-17
1.4	1.23817E-15	3.01982E-16

Table II: Power Delay Product Comparison of existing and proposed 2:1 multiplexer structure

V. APPLICATION OF PROPOSED 2:1 MULTIPLEXER IN LOW POWER AND HIGH PERFORMANCE ADDER CELL

A. Adder Circuit Using Existing 2:1 Multiplexer Circuit

Schematic of adder circuit using existing 2:1 multiplexer circuit is shown in Fig.8. This design of full adder circuit is based on three transistor XOR gates and

existing 2:1 multiplexer. In this circuit the (W/L) ratio for transistor T2 ,T5 are $(W/L)_n$=1/1 and

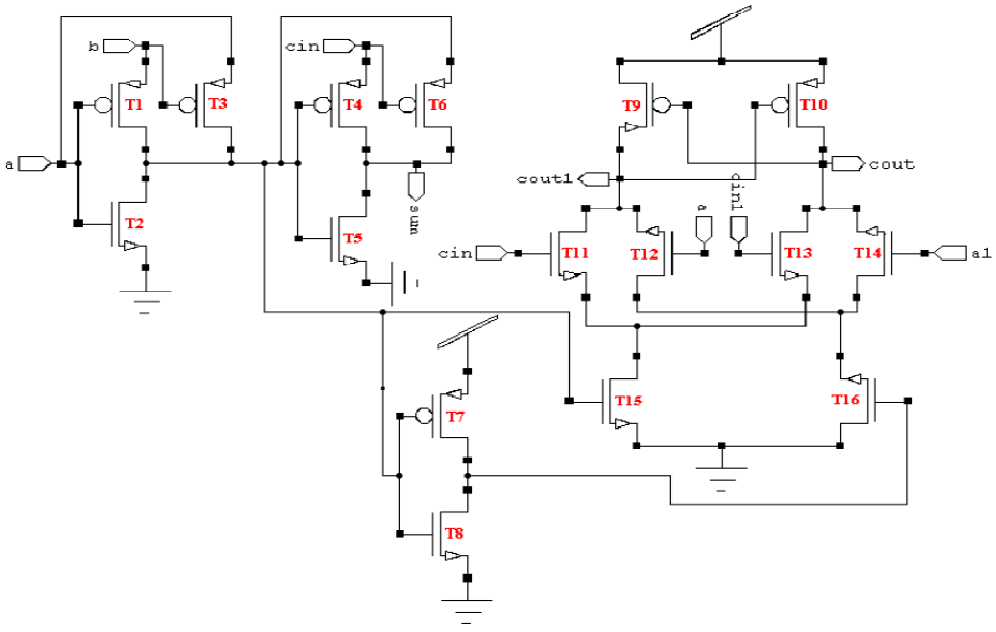

Fig. 8 : Schematic of adder circuit using existing 2:1 multiplexer

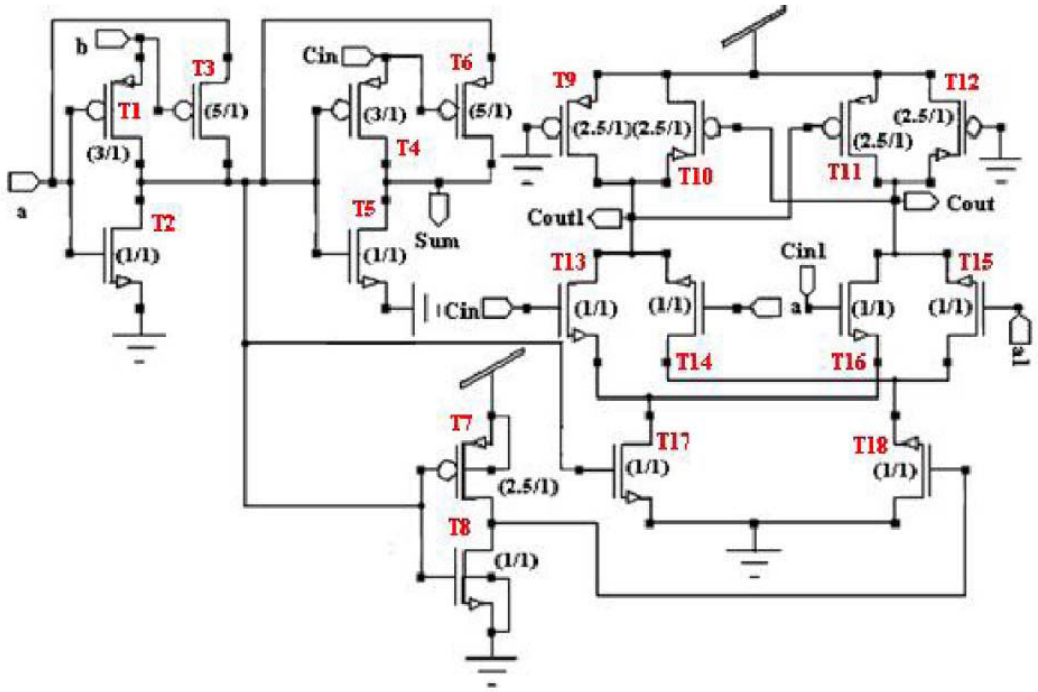

Fig. 9 : Schematic of adder circuit using proposed 2:1 multiplexer

B. Adder Circuit Using Proposed 2:1 Multiplexer Circuit

Schematic of Adder circuit using proposed 2:1 multiplexer circuit is shown in figure9.This design of full adder circuit is based on three transistor XOR gates and proposed 2:1 multiplexer [9], [10], [11]. The defined values of (W /L) for all transistors are same as the previous circuit. The Boolean equations for the design of this circuit are as follows:

$$Sum = A \oplus B \oplus CinCout = Cin(A \oplus B) + A \cdot (A \odot B)$$

VI. PERFORMANCE ANALYSIS

The graph shown in figure 10 - figure 12 reveals that the one bit full adder cell using proposed 2:1 multiplexer technology proves its superiority in terms of power, delay, power-delay product at varying supply voltages and temperatures over using existing 2:1 multiplexer technology. The graph shown in figure 10 reveals that the power consumption of proposed 2:1 multiplexer based one bit full adder cell circuit is remarkably reduced than the existing 2:1 multiplexer based one bit full adder cell at 45nm technology. The delay of the circuits is shown in figure11. Proposed 2:1 multiplexer based one bit full adder cell circuit shows slightly more delay than the delay of existing 2:1 multiplexer based one bit full adder cell for input voltage ranging from 0.6V to 1.4V. As it is found from the simulations proposed 2:1 multiplexer based one bit full adder cell shows better performance for the range of temperature as shown in figure12. Table III show the power delay product over a range of power supply voltages and as it is shown in the table that proposed 2:1 multiplexer based one bit full adder circuit show minimum power delay product.

V_{DD} (volts)	Power Delay Product(Watt-sec) (45nm)	
	Existing Adder	Proposed Adder
.6	7.88E-16	7.32E-16
.8	4.03E-15	3.37E-15
1	1.66E-14	9.39E-15
1.4	1.01E-13	4.09E-14

Table III: Power Delay Product Comparison of existing and proposed adder structure

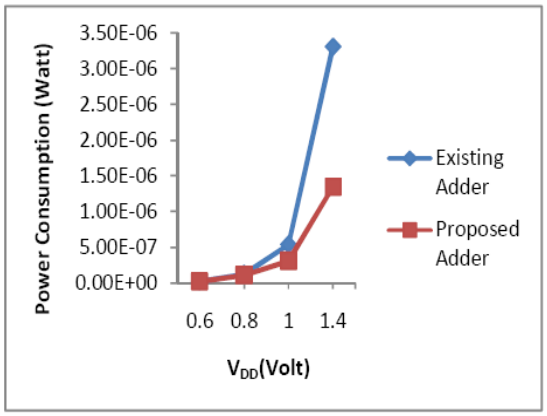

Fig. 10 : Power consumption comparison of existing and proposed adder cell at different supply voltages

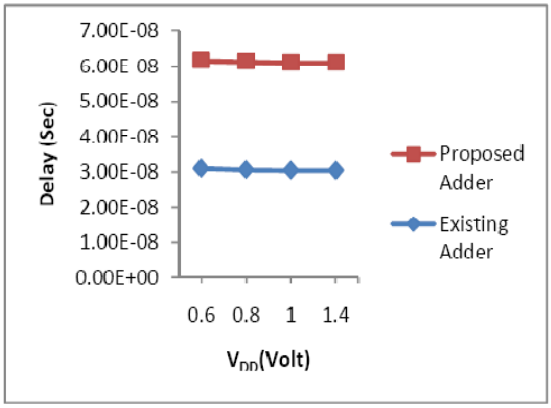

Fig. 11: Delay comparison of existing and proposed adder cell at different supply voltages

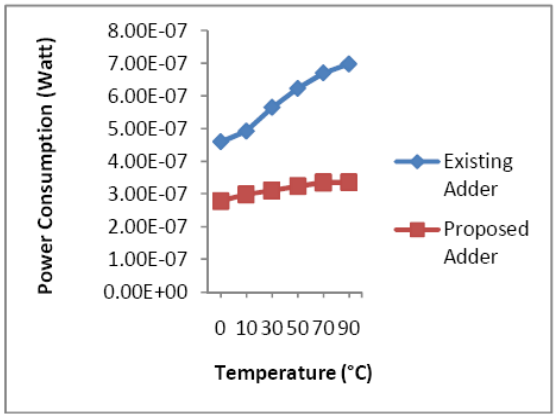

Fig. 12 : Power consumption comparison of existing and proposed adder cell at different temperatures

VII.CONCLUSION

For low-leakage and high-speed circuits concern should be on both the factors speed and power [12]. The proposed 2:1 multiplexer is found to give better performance than the existing 2:1 multiplexer. The proposed circuit has been tested to have better temperature sustainability, frequency and significantly less power-delay product to achieve high performance. The proposed 2:1 multiplexer has been designed and studied using 45nm technology and proved it to be a better option for low power complex system design. Also the proposed 2:1 multiplexer based 1-bit full adder is found to give better performance than the existing 2:1 multiplexer based full adder. It shows remarkable improvement in power delay product and has better temperature sustainability. The net effect is that proposed 2:1 multiplexer shows a much better performance compared to existing 2:1 multiplexer.

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Enhancement of Spectrum Efficiency for Cognitive Radios

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Abstract **-** Cognitive Radio (CR) remains strong as the communications community strives to solve the spectrum congestion problem. In existing work, Under the hierarchical DSA model, interactions between primary and secondary users are considered to achieve spectrum efficiency. The overlay/underlay waveform that realizes both waveforms and demonstrated its performance in an AWGN channel. The drawbacks are Spectrum congestion, Inefficient usage of channel, High power spectrum and Interference to users. In this paper, Analysis is done and the performance of the proposed hybrid overlay/underlay waveform in multipath fading channels is evaluated. This was done by extending the original Spectrally Modulated Spectrally Encoded (SMSE) framework to enable soft decision CR implementations that exploit both unused (white) and underused (gray) spectral areas. It avoids spectrum congestion and fading effects. Finally, the benefits of combining overlay/underlay techniques which enhances the spectrum efficiency and maximizes the channel capacity is addressed.

Keywords **-** *Software defined radio, cognitive radio, noncontiguous waveform, overlay waveform, underlay waveform, dynamic spectrum access.*

I. INTRODUCTION

SPECTRUM overcrowding continues to present a fundamental challenge for both military and commercial communications as earlier concerns over spectrum congestion and inefficient usage [1] of the channel. A number of Dynamic Spectrum Access (DSA) models have been proposed to enhance the spectrum efficiency. Under the hierarchical DSA model, interactions between primary and secondary users are considered to achieve spectrum efficiency [2], [3]. Thus, the hierarchical DSA model is synonymous with Cognitive Radio (CR) technology. In current CR research, the secondary user may use either an *overlay* waveform to harness unused spectrum holes (white areas) and avoid interference to the primary users, or an *underlay* waveform to spread its energy across a very wide bandwidth with very low power spectrum density such that interference to primary users is minimized.

In previous work a hard decision CR design that realizes benefits of both overlay and underlay waveforms [4]. As demonstrated for a non-faded AWGN channel, the proposed waveform effectively exploits both unused spectrum holes and underused spectrum bands to improve overall channel capacity and Bit Error Rate (BER) performance of the secondary user, without impacting the primary users' transmission. Specifically, the work in [4] extended the original Spectrally Modulated Spectrally Encoded (SMSE) framework in [5]–[7] to create a soft decision SMSE (SD-SMSE) framework [8], [9] that supports a group of multi-carrier based signals to generate hybrid overlay/underlay waveforms in support of soft decision CR applications. The BER of overlay, underlay and hybrid overlay/underlay CR waveforms was the primary evaluation metric.

The original SMSE framework [5] provides a unified expression for generating and implementing a host of multicarrier waveforms (e.g., OFDM [10], MC-CDMA [11], CI/MC-CDMA [12], [13], TDCS [14], [15], etc) and satisfies current CR goals of exploiting unused spectral bands. However, the original work did not explicitly exploit *underused* spectrum. Here, extended the original SMSE framework into a soft decision SMSE (SD-SMSE) framework by relaxing conditions on the binary (hard decision) spectrum *availability* variable **a** to allow for assignment of real values (soft decision), i.e.,

$$a = \left[a_{0,}\, a_{1,\ldots,} a_{N-1} \right] \quad 0 \le a_m \le 1 \qquad (1)$$

A new design variable, b, was also introduced to allow exploitation of *underused* spectrum,

$$b = [b0,\ b1,\ \ldots,\ bN-1] \qquad (2)$$

where,

$$b_m = \{0 \quad a_m = 1$$

$$a_m \; a_m \neq 1 \qquad (3)$$

Fig.1 : Block diagram representation of Overlay with channel coding.

Accounting for *unused* spectrum through vector **u** and *underused* spectrum through vector **b**, the discrete time domain waveform for a general soft decision CR waveform can be expressed as:

$$S_K[n] = \frac{1}{N} Re\{\sum_{m=0}^{N-1} u_m \; c_m \, d_{m,k} w_m \qquad (4)$$

$$.e^{j(2\pi f_m t_n + \theta d_{m,k} + \theta c_m + \theta w_m + \theta o_{m,k})}\}$$

$$+\frac{1}{N} Re\{\sum_{m=0}^{N-1} b_m c_m d_m, k w_m$$

$$.e^{j(2\pi f_m t_n + \theta d_{m,k} + \theta c_m + \theta w_m + \theta o_{m,k})}\}$$

Where terms in the first summation of (4) account for *unused* frequency components and terms in the second summation account for *underused* frequency components.

In Part I ,demonstrated that the SD-SMSE framework can be used to effectively generate overlay CR waveforms (such as NC-OFDM, NC-MC-CDMA, NC-CI/MC-CDMA and NCTDCS), underlay CR waveforms (such as Multiband OFDM UWB), and hybrid overlay/underlay waveforms and evaluated each of their performances in an AWGN channel [4]. For one realization, here combined hybrid overlay/underlay waveform design with channel coding and demonstrated excellent performance. As shown in Fig. 1 and Fig. 2, the hybrid overlay/underlay approach is combined with systematic block channel coding where the information bits are transmitted via overlay waveform (over unused frequency bands), and the redundant bits are transmitted via underlay waveform (over *underused* frequency bands). This way, both the *unused* and the *underused* frequency bands are utilized. Compared to pure overlay system, the new overlay/underlay system exploits channel coding gain without sacrificing data rate. More importantly, the overlay/underlay system possesses an increased degree of flexibility in receiver design. If preferred, no channel decoding needs to be implemented and the receiver simply demodulates the data from the overlay transmission. On the other hand, with a channel decoder present the overlay/underlay receiver can improve the performance significantly.

In this paper I analyze and evaluate BER performance of overlay, underlay and hybrid overlay/underlay waveforms in multipath fading channels. As demonstrated through simulation, the hybrid overlay/underlay waveforms exhibit superior performance over frequency selective fading channels

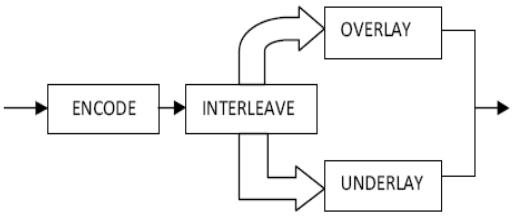

Fig. 2 : Hybrid overlay/underlay technique using channel coding

When compared with both conventional overlay and underlay waveforms. The remainder of this paper is organized as follows: Section II analyzes and derives BER performance of overlay and underlay waveforms for frequency selective fading channels. Computer simulation results are presented in Section III followed by conclusions in Section IV.

II. PERFORMANCE ANALYSIS IN MULTIPATH FADING CHANNELS

The analytic expression to evaluate the BER performance of overlay and underlay waveforms in multipath fading channels is derived here,the total received signal in a CR scenario is

$$r(t) = \sum_{k=1}^{K} rp_k(t) + \sum_{l=1}^{L} r_{sl}(t) + n(t) \qquad (5)$$

where as before K is the total number of primary users, L is the total number of secondary users, r_{pk} (t) represents the received signal of the k_{th} primary user, r_{sl} (t) is the received signal of the l_{th} secondary user, and $n(t)$ represents AWGN having a two-sided power spectrum density of $N0/2$.

After transmission through a multipath fading channel with impulse response *h(t),* the received secondary user signals are given by

$$r_{sl}(t) = h(t) * s_{sl}(t) \qquad (6)$$

Where $s_{sl}(t)$ is the l^{th}*secon*dary user's transmitted signal.

Assuming that the k_{th} primary user transmits an OFDM signal with BPSK modulation over M_k subcarriers, the transmitted signal for the k_{th} primary user is obtained.

A. Performance Analysis of Overlay Waveforms

When the secondary user employs an overlay waveform for transmission, only spectrum holes are used. Here, it is assumed that one secondary user is transmitting over all the available spectrum holes. The received signal corresponding to the secondary user waveform employing NC-OFDM. Similarly, the received signal of a secondary user employing NC-MC-CDMA. Given that primary and secondary user transmissions are assumed to be synchronized in time, and the secondary user only transmits within spectrum holes, there is no interference from the secondary user to primary users and vice versa. The corresponding average BER *P(e)* is calculated using

$$P(e) = \int_0^\infty Q\left(\sqrt{SINR}\right)p(SINR)d(SINR) \qquad (7)$$

where $p(SINR)$ is the probability density function of SINR. The expression can be determined via numerical methods which can be easily implemented.

B. Performance Analysis of Underlay Waveforms

When underlay waveforms are employed by secondary users their transmissions occupy the entire available bandwidth instead of just the spectrum holes. Here, multiple secondary users can be accommodated using MC-CDMA with the composite secondary users' signal. At the receiver, the received signal is first decomposed into N subcarrier components and then recombined to create the final decision variable for the desired secondary user. When one subcarrier exists in a spectrum hole, there is no primary user signal contribution at that subcarrier.

However, if at least one secondary user subcarrier is not within a spectrum hole, the secondary users' signal spectrally coexists with one primary user's signal.After frequency combining, the final decision variable corresponds to:

$$R^{(n)} = \sum_{i=0}^{N-1} W_i . r_i^{(n)}$$

$$= \sum_{i=0}^{N-1} W_i \alpha_i \sqrt{\frac{E_{b_S}}{N}}\ b^{(n)} \qquad (8)$$

$$+\ \sum_{i=0}^{N-1} W_i \alpha_i \sqrt{\frac{E_{b_S}}{N}} \sum_{l=1, l\neq n}^{L} b^{(l)} \beta_i^{(l)} \beta_i^{(n)}$$

$$+\sum_{k=0}^{K} \sum_{i\in P_k} W_i\ \alpha_i' \sqrt{E_{b_k}}\ b_i^{(k)}$$

$$+\sum_{i=0}^{N-1} W_i n_i$$

where P_k is the subcarrier set of the k_{th} primary user. It is relatively straightforward to show that the instantaneous SINR is given by

$$\text{SINR} = \frac{P_{Signal}}{P_{MAI}+P_{PUI}+P_{Noise}} \qquad (9)$$

$$\text{SINR} = \left\{\frac{E_{b_S}}{N}\left(\sum_{i=0}^{N-1} W_i \alpha_i\right)^2\right\} /$$

$$\left\{(L-1)\frac{E_{b_S}}{N}\sum_{i=0}^{N-1} W_i^2 \alpha_i^2 + \sum_{k=1}^{K}\sum_{i\in P_k} W_i^2 \alpha_i'^2 E_{b_k} + \frac{N_0}{2}\sum_{i=0}^{N-1} W_i^2\right\}$$

with the corresponding BER

III. SIMULATION RESULTS

Performance overlay, underlay and hybrid overlay/underlay waveforms is demonstrated via simulation over a frequency selective fading channel. Analytic and simulated P_b versus E_b/N_0 are used as performance metrics to validate waveform performance.

To model a realistic wireless channel, a Rayleigh fading channel is employed in the simulations to induce frequency selectivity across the available bandwidth BW. However, only flat fading is induced on each individual subcarrier. The simulations assume a channel model with coherence bandwidth of Δf_c being eight times the subcarrier bandwidth , i.e. $\Delta f_c = 8\Delta f$. Hence, a primary user that transmits over $N_p = 32$ subcarriers observes 4-fold diversity and in the overall CR bandwidth of 64 subcarriers the frequency selectivity is 8 folds. To mitigate multipath fading effects and take maximum advantage of the diversity, a minimum mean square error combining (MMSEC) diversity approach is used.

A. Simulation Analysis of Overlay waveform in Multipath Fading

In this section, performance of overlay-CR waveforms in frequency selective fading channel is demonstrated. The overlay spectrum allocation scenario is assumed to have $N = 64$ total available subcarriers, with $N_p = 32$ subcarriers allocated to the primary user and $N_{CR} = 32$ allocated to the overlay-CR user at any given time. It is also assumed that the primary user signals, which are modeled as OFDM-BPSK, are not passing through a fading channel. As noted, the primary and secondary users are perfectly time synchronized. Results in Fig.2 illustrate frequency selective fading channel performance of OFDM with BPSK and MC-CDMA with BPSK, respectively, as obtained using the MMSEC diversity combining technique for MC-CDMA system. It is clearly evident in the figure that as the number of subcarriers increases, the performance gain for MC-CDMA system due to frequency diversity also increases. It is also worth noting that the difference in performance improvement increases at higher E_b/N_0 values. As shown in Fig. 2, the simulation results for

N=128 close matches the analytic results, validating assumptions made in deriving the analytic expression as well as in the implementation.

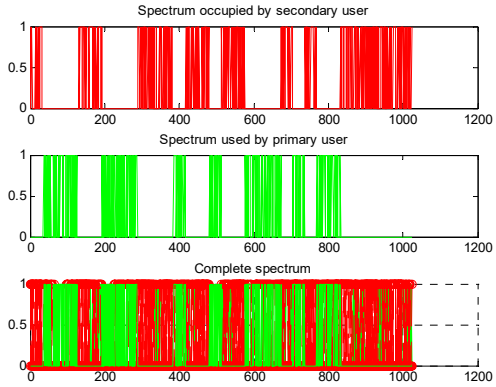

Fig. 1: It shows the complete spectrum occupied by primary and secondary user.

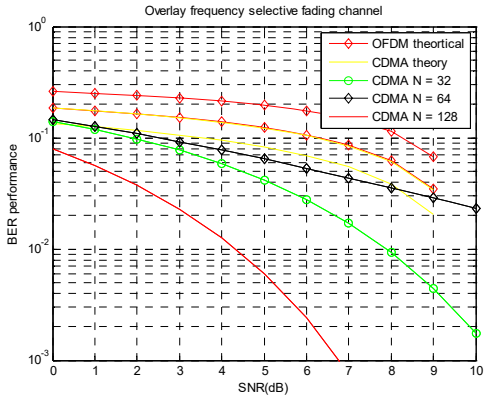

Fig. 2

B. Simulation Analysis of Underlay Waveform in Multipath Fading

Simulation results are presented to demonstrate underlayCR waveform performance in a frequency selective fading environment. The underlay-CR waveform employed by the secondary user either occupies the entire CR bandwidth or some lesser amount of bandwidth depending on data rate and interference requirements set forth by the primary users. In overlay-CR waveform implementation and analysis, perfect time synchronization was assumed between primary and overlay-CR secondary users. However, in underlay-CR analysis primary and secondary waveforms overlap temporally and spectrally which effectively increases SINR in both systems.To minimize the mutual interference, underlay waveforms perform similar to UWB and spread spectrum signals and are expected to operate under the noise floor of primary user signals.

The frequency selective channel model used for overlay-CR simulation remains unchanged for underlay-CR analysis and simulation. Recall that these simulations assumed four-fold frequency diversity in the N_{CR} = 32 subcarrier bandwidth. As the bandwidth increases due to underlay-CR waveform spreading, the number of diversity folds also increases which results in performance improvements provided by utilizing an appropriate diversity combining technique. Results in Fig. 3 to Fig. 6 illustrate performance for an underlay-CR waveform employing MC-CDMA with BPSK modulation. The underlay-CR waveforms are assumed to be operating at -20 dB relative to the primary user. Each of the primary users is modeled as using N_p = 32 subcarriers with OFDM and BPSK modulation. MMSEC combining technique is employed in these systems. The BER performances in different scenarios are compared in these figures, and also compared with the analytical BER performance. It is obvious

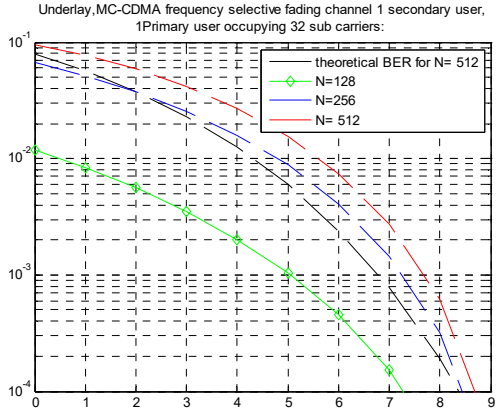

Fig.3

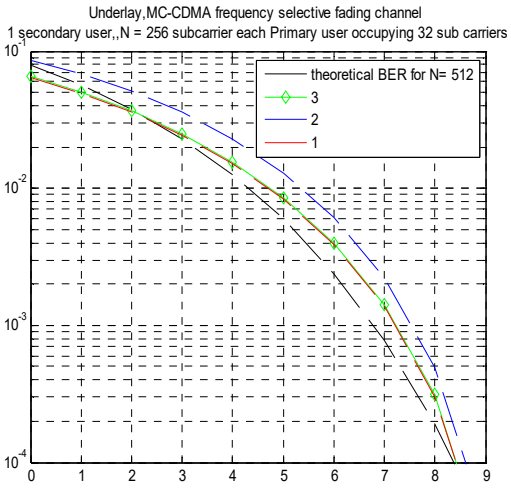

Fig. 4

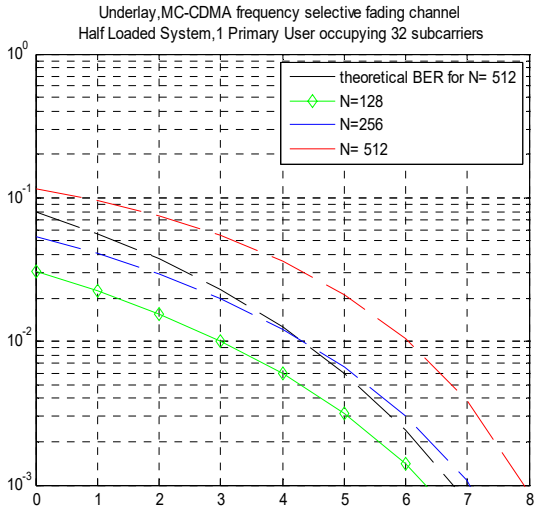

Fig. 5

that the BER performances match the analytic results perfectly. Fig. 4 and Fig. 5 illustrate the BER performance for a different number of total subcarriers $\mathcal{N}$. In both systems, there is one primary user occupying $\mathcal{N}_p$ = 32 subcarriers. In Fig. 4, there is only one secondary user, while Fig. 5 applies a half loaded system. It is evident that by increasing the number of subcarriers, there is performance improvement due to the diversity gain.

IV. CONCLUSION

To enhance the spectrum efficiency and to improve the channel capacity both *unused* (white) and *underused* (gray) spectral regions need to be exploited. Using a previously developed SMSE framework based on hard decision spectrum usage, an extended soft decision SMSE framework (SDSMSE) is developed to support soft decision CR applications using Rayleigh faded channels. A complete spectrum is shown which eliminates the interference to the users. The SD-SMSE CR implementation is capable of dynamically generating spectrally efficient overlay, underlay and hybrid overlay/underlay waveforms. Performance is evaluated here for all the SDSMSE waveform types in the CR context over multipath fading channels.

ACKNOWLEDGMENT

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Wireless Authentication with Elliptic Curve Cryptography Based on ARM7

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Abstract - In this paper, we present the results of our implementation of elliptic curve cryptography (ECC) on an 80-MHz, 32-bit ARM microprocessor. We support variable length implementation of the elliptic curve digital with recently proposed ECC-based wireless authentication protocol. Our timing result shows that the 160-bit ECDSA signature generation and verification operations take around 46 ms and 94 ms, respectively. With these timings, the execution of the ECC-based wireless authentication protocol takes around 140 ms on the ARM7TDMI processor, which is a widely used, low-power core processor for wireless applications.

Keywords - *ECC, ARM 7 TDMI processor, ECDSA, RSA, SHA.*

I. INTRODUCTION

Public-key cryptography offers robust solutions to many of the existing problems in communication systems, however, excessive computational demands (on-line memory, code size, and speed) have made the use of public key cryptography limited, particularly on wireless communication systems. Elliptic curve cryptography [27, 23, 13] offers secure and efficient solutions for the new communication technologies.

It requires fewer bits than the RSA for similar amount of security. Certicom's SigGen smartcard [14] is an example ECC software implementation on a restricted platform. It is a prototype smartcard with an 8-bit microprocessor that generates digital signatures using a conventional core from Motorola(68SC28). They are generated in less than 600 ms while using only 90 bytes of RAM. It has been implemented in less than 4K code to support the RSA. They have reported a speed of 150 ms for generating a 160-bit ECDSA signature and 630 ms for verifying the signature. Total code size was 4 kilobytes, including the SHA-1. There are much faster implementations of the ECC [21].The algorithms which are necessary are wireless authentication protocol described in [10]. We implemented the protocol on the 32-bit ARM7TDMI microprocessor using the low-power wireless communication platforms [16,17]. In our implementation, we obtained the timings of 46.4ms ECDSA signature generation and 92.4 ms ECDSA signature verification for the 160-bit ECC.

II. DESCRIPTION

The drafted IEEE standard [20] proposes the use of the fields GF(p) and GF(2k). The use of the field GF(p) requires that we implement modular arithmetic with respect to the prime modulus p. Due to the security requirements, the size of p is at least 100 bits, usually around 160 bits. The large number arithmetic has been extensively studied in the context of the RSA algorithm, and efficient algorithms for field multiplication have been designed [24]. An efficient method for performing the field multiplication is the Montgomery method [28, 25], which effectively performs modulo 2k multiplication instead of modulo p multiplication.

III. ELLIPTIC CURVE DIGITAL SIGNATURE ALGORITHM

The operations in the elliptic curve analogue of the Digital Signature Algorithm utilize the arithmetic of points which are elements of the set of solutions of an elliptic curve equation defined over a finite field. The security of the protocol depends on the intractability of the elliptic curve analogue of the discrete logarithm problem. First, an elliptic curve E defined over GF(p) with large group of order n and a point P of large order is selected and made public to all users. Then, the following key generation primitive is used by each party to generate the individual public and private key pairs. Furthermore, for each transaction the signature and verification primitives are used. We briefly outline the

Elliptic Curve Digital Signature Algorithm (ECDSA) below, details of which can be found in [19].

In the ECDSA Key Generation user A follows these steps:

1. Select a random integer d ∈ [2, n − 2].
2. Compute Q = d × P.
3. The public and private keys of the user A are (E,P, n,Q) and d, respectively.

User A signs the message m using the following steps.

1. Select a random integer k ∈ [2, n − 2].
2. Compute k × P = (x1, y1) and r = x1 mod n. If x1 ∈ GF(2k), it is assumed that x1 is represented as a binary number. If r = 0 then go to Step 1.
3. Compute k−1 mod n.
4. Compute s = k−1(H(m) + d · r) mod n.

   Here H is the secure hash algorithm SHA.

   If s = 0 go to Step 1.
5. The signature for the message m is the pair of integers (r, s). ECDSA Signature Verification for the user B verifies A's signature (r, s) on the message m by applying the following steps:

1. Compute c = s−1 mod n and H(m).
2. Compute u1 = H(m) · c mod n and u2 = r.c mod n.
3. Compute u1 × P + u2 × Q = (x0, y0) and v = x0 mod n.
4. Accept the signature if v = r.

IV. HARDWARE DESCRIPTION

The present work is implemented using ARM 7 TDMI and the necessary embedded C program is developed and dumped into the embedded processor using Flash magic ISP Utility. The ARM 7 TDMI allows you to develop and manage complete embedded application projects [13]. In-System Programming is programming or reprogramming the on-chip flash memory, using the boot-loader software and a serial port. The block diagram of LPC2387 microcontroller as shown in fig.1 is based on a 16-bit/32-bit ARM7TDMI-S CPU with real-time emulation that combines the microcontroller with 512 kB of embedded high-speed flash memory. A 128-bit wide memory interface and unique accelerator architecture enable 32-bit code execution at the maximum clock rate. For critical performance in interrupt service routines and DSP algorithms, this increases performance up to 30 % over Thumb mode. For critical code size applications, the alternative 16-bit Thumb mode reduces code by more than 30 % with minimal performance penalty.

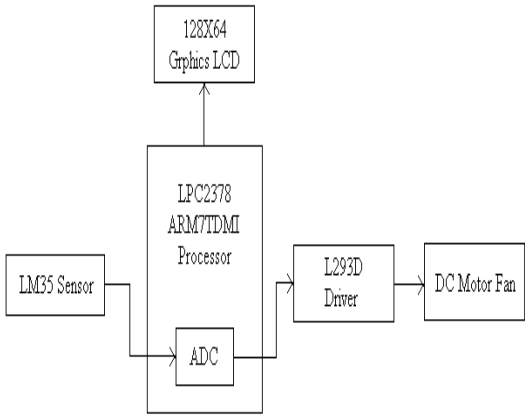

Fig. 1 : Block diagram.

The LPC2387 is ideal for multi-purpose serial communication applications. It incorporates a10/100 Ethernet Media Access Controller (MAC), USB full speed device with 4 kB of endpoint RAM, four UARTs, two CAN channels, an SPI interface, two Synchronous Serial Ports (SSP), three I2C interfaces, and an I2S interface. This blend of serial communications interfaces combined with an on-chip 4 MHz internal oscillator, 64 kB SRAM, 16 kB SRAM for Ethernet, 16 kB SRAM for USB and general purpose use, together with 2 kB battery powered SRAM makes this device very well suited for communication gateways and protocol converters. Various 32-bit timers, an improved 10-bit ADC, 10-bit DAC, one PWM unit, a CAN control unit, and up to 70 fast GPIO lines with up to 12 edge or level sensitive external interrupt pins make this microcontroller particularly suitable for industrial control and medical systems.

The LPC2378 Microcontroller provides on-chip boot-loader software that allows programming of the internal flash memory over the serial channel [5]. Philips provides a utility program for In-System programming called Flash magic Software [6].

V. RESULTS AND CONCLUSIONS

Embedded ARM processor based temperature sensing requires that the temperature of the high speed chip should be first measured. This is done by placing a temperature sensor close to the target chip either directly next to it or in some cases, under it or on the heat sink. The temperature measured in this way corresponds to that of the high speed chip, but can be significantly lower and the difference between measured temperature and the actual die temperature increases as the power dissipation increases. So, the temperature of the circuit

board or heat sink must be correlated to the die temperature of the high speed chip [7]. Of course a better alternative is possible with a number of high speed chips. This not only eliminates the large temperature gradients involved in measuring temperature outside the target IC's package, but it also eliminates the long thermal time constants, from several seconds to minutes, that cause delays in responding to die temperature changes.

In some systems, it is also important to limit the rate of change of the fan speed. This is critical when the system is in close proximity to users. Simply switching a fan on and off or changing speed immediately as temperature changes is acceptable in some environments. But when users are in nearby, the sudden changes in fans noise are highly annoying. So to avoid these effects the fan's drive signal must be limited to an acceptable level. Possible enhancements for further speeding up and/or reducing the code size are:

- The scalar multiplication of the base point can be performed in more efficient way by having a precomputed look-up table in ROM area.
- The finite field multiplication operations dominate the performance of signature generation and verification. Even a small improvement on the existing multiplication routine improves the overall ECDSA performance.
- The 16-bit wide Thumb instruction set of ARM7TDMI can be used to reduce the code size.

VI. FUTURE SCOPE OF THE WORK

In the present work, we can use a remote diode temperature sensor connected to the thermal diode which measures the temperature of the high speed ICs directly with excellent accuracy. The first IC can sense the remote temperature and controls the fan speed based on that temperature [8]. It produces a DC supply voltage for the fan through an internal power transistor. The second IC also performs a similar function but drives the fan with a PWM waveform through an external pass transistor. Both include complete thermal fault monitoring with over temperature outputs, which can be used to shut down the system if the high speed chips get too hot. So, the present work can be improved further by using the above mentioned techniques.

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Bi-directional Energy Meters for Smart Grid Applications Using LonWorks Technology

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Abstract - This paper discusses the implementation of bi-directional smart energy meter based on the LonWorks technology. A smart meter is an electrical device that records consumption of electrical energy and various other electrical parameters and enables the measurement of energy in both directions (export and import). This digital energy meter has the Neuron processor as the central controlling unit. The Neuron chip is a VLSI chip that makes it possible to implement low-cost local operating network applications. This neuron chip is interfaced with energy metering chip and this is termed as the energy node. The energy metering chip facilitates bidirectional energy measurement i.e., it can be programmed to measure both Import and Export energy. The application program is written in Neuron C to read data through the SPI bus, calculate & scale the data to the required engineering unit. Then the data is converted to the Standard Network Variable Type (SNVT). Further this energy node is interfaced with the iLON Smart Server, which has inbuilt data loggers and schedulers and programmable interfaces. This server allows us to link many devices to it. Not only can we access and monitor these devices, but also use the captured data for efficient energy management. The smartness of the system lies in its bidirectional energy measurement capability, interoperability, compactly sized energy nodes with aesthetic display and to be interfaced with a web server making it a web based monitoring system which can be used for remote management applications

Keywords - *Energy node, LonWorks Technology, Bi-directional energy measurement, Neuron processor and iLon Smart Server.*

I. INTRODUCTION

Smart meter is an advanced digital energy meter. It measures consumption of electrical energy and also provides information about a multitude of electrical parameters- voltage, current, active and reactive power, power factor. Integration of smart meters into electricity grid involves implementation of a variety of techniques and software, depending on the features that the situation demands. Design of a smart meter depends on the requirements of the utility company as well as the customer. [2]

Measurement of energy requires a metering device. The existing meters are mostly unidirectional in the sense that they measure either only the export or the import energy at one instance. The meter proposed and developed in this paper, utilizes the bi-directionality feature of the energy metering chip to implement a system that measures the import and export energy. A single node keeps track of energy consumed and energy generated. Bi-directional energy measurement is an important feature of a smart meter for active collaboration of power provider and power user.

II. HEART OF THE SYSTEM – LONWORKS

The energy meter discussed has its base with the LonWorks technology. LonWorks is the name of the control networking technology platform and not just a protocol. It uses the flat peer to peer architecture. In P2P, no single master on the network determines if a message from one device should be sent to another, nor determines in what order messages should be sent. Instead, control devices are free to communicate directly with each other; this reduces bottlenecks and prevents the system wide failures that can occur when the master fails. As a result, P2P-based control networks offer high reliability and high performance.

A. THE SYSTEM

The energy metering system consists of the energy node (smart meter) which is interfaced with the iLON Smart Server .The server can then be connected to a PC for monitoring of nodes. The nodes can also be individually connected to a computer using a twisted pair for communication. The communication between the energy node and the server is also through a twisted pair cable. Many number of nodes can be connected to the server and can be continuously monitored.

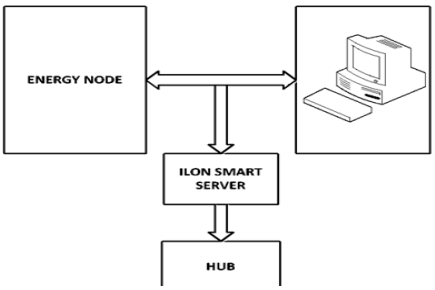

Fig.1 : Block Diagram of the Metering System

B. MASTER – THE NEURON CHIP

The entire energy node is controlled by the neuron processor. The neuron chip is a VLSI device that makes it possible to implement low-cost operating network applications. The neuron chip has a combination of hardware and firmware that can receive values from the sensors, process them and propagate control information across the network. The neuron chip is programmed using the NEURON C programming language. [3]

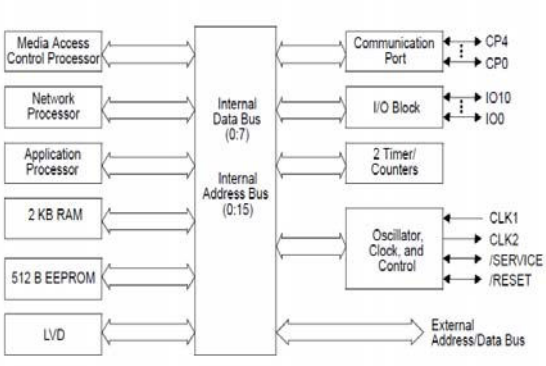

Fig.2: Block Diagram of the Neuron Chip [3]

C. THE ENERGY METERING CHIP

The most significant feature of the energy metering chip is the ability to adapt to the flow of energy in either direction. The chip has an in-built 24bit registers. These registers receive sampled data in the digital form that represent the active and reactive power consumed and various other electrical parameters. These 24bit registers increment during the positive energy flow and decrement during the negative energy flow. [5] This energy metering chip board has current and potential transformers and voltage and current sense resistors. The transformers are used to step down the three phase voltages and currents to the rated values that can be supported by the chip. The chip is also self protected against ESD (electro static discharge).

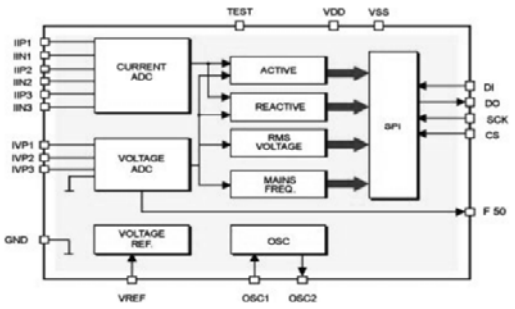

Fig. 3 : Block Diagram of the Energy Metering Chip

D. THE ENERGY NODE

The interfacing of the neuron chip with the energy metering chip and a display forms the energy node. This is a standalone system that is used to provide readings of all the electrical parameters. The neuron chip communicates with the energy metering chip with the SPI bus. The neuron processor has three, eight bit pipelined processors two of which are dedicated to communications and the third to applications task.

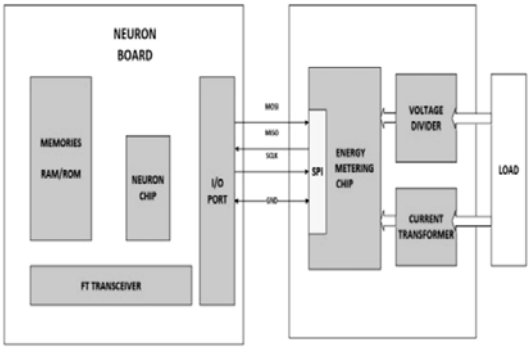

Fig.4 : Block Diagram of the Energy Node [1]

E. BI-DIRECTIONALITY IMPLEMENTATION AND TESTING

The behaviour of the energy metering chip differs during the positive and the negative flow of energy. The 24bit registers increment during the positive (import) and decrement during the negative (export) flow of energy. The values of these registers are continuously monitored by the neuron chip. The neuron chip is so programmed that it can track both the increment and decrement of the registers, thereby separating the import and export energy. Successive differences in the register values are operated upon by the neuron chip to provide instantaneous values of power. The power values of the three phases are used to compute the total energy accumulation. There are separate network variables assigned, that govern the total energy accumulation, the

export energy and the import energy. The register values of the energy meter are taken and calculated using several formulae. The metering chip's registers wrap around approximately every 52 seconds. So appropriate wrap around correction is provided in the neuron chip program lest it leads to wrong difference value. The active and reactive power registers increment or decrement at 320 kilo samples per second and this is taken into account while calculating the energy per count. The node is programmed using Neuron C programming language. The parameters that are monitored on the browser are declared as network variables. The register values are read from the energy metering chip by the processor through the SPI bus. The data so obtained is operated upon to obtain the values of various electrical parameters, which are converted to Standard Network Variable Types (SNVT). The values are monitored on the LonMaker for Windows Browser. The input network variables like CT ratio and PT ratio, calibration coefficients can be set in the field during installation.

The node is implemented in the following way:

a. **If energy flow is positive**

a1. Check for wrap around and do correction if required

a2. Calculate power for each phase and active energy

a3. Increment total energy variable and import energy variable

b. **If energy flow is negative**

b1. Check for wrap around and do correction if required

b2. Calculate power for each phase and active energy

b3. Increment total energy variable

The wrap around happening in the active and reactive power registers is corrected by either adding or subtracting the full scale register value to the presently calculated active or reactive power differences, depending on whether energy is imported or exported.

The total energy variable **en_w_total** increments irrespective of the flow direction.

The import energy variable **en_w_import** increments only during positive flow.

The export energy value, **en_w_export** is obtained from the difference between **en_w_total** and **en_w_import**.

The test results are tabulated in the table 1 for various power factors with a voltage of 240V and a current of 5A .The node was tested using CALSOURCE 200, a three phase source with provision to vary the load currents and power factors.

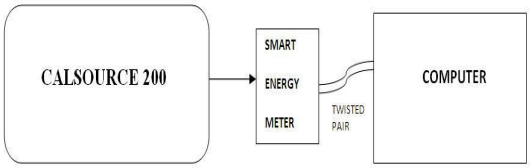

Fig. 5 : Block Diagram of an energy node connected to a computer for testing

TABLE 1

TEST RESULTS

Total energy (Whr) (en_w_total)	Export Energy (Whr) (en_w_export)	Import Energy (Whr) (en_w_import)	Accumulation between time instants (Whr)
8620	3034	5586	0(0 MINUTES)
8922	3336	5586	302(5MINUTES)
9223	3637	5586	301(10MINUTES)
9523	3937	5586	300(15MINUTES)
9825	4239	5586	302(20 MINUTES)
9953	4336	5617	0(0 MINUTES)
10256	4336	5920	303(5MINUTES)
10554	4336	6218	298(10MINUTES)
10855	4336	6519	301(15MINUTES)
11154	4336	6818	299(20 MINUTES)

F. INTERFACING WITH THE SMART SERVER

The energy node developed and tested above is connected to the iLON Smart Server. This server has inbuilt data loggers and schedulers that store and retrieve the data from the node. The server has the advantage that a large number of nodes can be connected at the same time and monitored as well. Smartness of this system is further enhanced by the fact that the iLON Smart Server can be interfaced to IP based applications. The energy meters connected to the server can be monitored and remotely configured.

III. CONCLUSIONS

The smart meter is one of the important features of a smart grid. The smartness of the digital energy meter is improved by the bi-directional energy measurement, the display, the server and on the whole the light weight

and its compatible size. This paper discusses in detail the technique for bi-directional energy measurement and its interoperability. Remote monitoring also is the need of the day to meet the features of smart grid requirements. The developed meter on interfacing to the smart server achieves this capability.

ACKNOWLEDGMENT

We sincerely thank all the scientists of CSIO Madras for encouraging and helping us in pursuing this project.

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Effective Test Case Creation For Software Testing

Daivik Bhatt[1], Amit Deepu[2] & Krunal Barot[3]

[1&2]Igate Patni Computer System, [3]Persistent System

Abstract - This paper describes an effective approach toward black-box testing. Black-box test cases are identified from functional requirements of the test system, which is viewed as a mathematical function mapping its inputs onto its outputs. . An effective set of test cases is the one that has a high probability of detecting faults presenting in a computer program. Identifying effective test factors is not only reducing the number of test cases but also increases the probability to detect more defects. In this paper, we introduce the concept of pairwise testing and algorithm to generate effective test set.

Keywords - *Pairwise testing, Test factors, Test case generation, Interaction failure.*

I. INTRODUCTION

Software reliability is often expressed by comparing the number of errors detected by testing with statistical data. In 'black-box test' method, test cases are designed from external specifications. To date, several black-box oriented test case design methodologies (e.g. 'equivalence partitioning', 'boundary value analyses, 'cause-effect graphing') [1] have been devised. These methodologies, however, do not solve all the problems encountered during black box testing. The followings are the examples of the problems which need to be solved:

- The input conditions must be extracted before equivalence partitioning and boundary value analysis can be used: these methodologies do not provide a means of extraction the input conditions from the external specifications alone.
- Cause- effect graphing requires a method to find out the relationship between causes and effects, but since there are no effective methods, it can hardly be extended to large-scale software in its present form.

The growing size of software and increasing complexity of relationship between software have also caused the need to consider the followings:

- Testing large-scale software requires a wide knowledge, including component programs and hardware.
- In tests involving many inspectors, a means is essential to standardize the quality of testing conducted by each inspector, but there is a limit as to the extent to which one can share the knowledge and skill through training.

To solve these problems, in addition to the methodologies of test case design, the system which allows each individual to share these knowledge and test cases to keep the standard quality must be constructed.

Over the years, a number of combinatorial strategies (e.g. random testing [4], each-choice and base-choice [2] and anti-random [3]) have been devised to help testers choose subsets of input combinations that would maximize the probability of detecting defects.

II. TEST CASE DESIGN PROCEDURE

Test case design follows these steps:

1. Division of function:

The functions are divided into smaller logical segments to create an outline for the test case design operations to follow. This procedure is called test classification.

2. Identification of test factors:

The input condition and their values are analyzed based on external specifications of each segment of the test functions. This procedure is called test factor analysis

3. Generation of test cases:

Test cases are generated by combining the possible values of input condition in the test factor table. This procedure is called test case generation.

4. Definition of test results:

Expected results of each generated test cases are entered in a test results description table.

III. PROBLEM IN TEST CASE DESIGN

Figure 1 gives the reasons for failure to detect errors in products prior to their shipment. The omission of test cases during test factor analysis is often associated with problems relating to the scope of knowledge and insight of the testing personnel, such as the following:

- Inadequate consideration of the internal operation factors not visible from external specifications.
- Inadequate consideration of the operation factors of other products related to the product under test.

The omission of test cases during test case generation is often caused by omission or careless errors during the process in which many test factors are implemented. Two of these factors are as follow:

- Omission of test factor combinations.
- Failure to include analyzed test factors as test cases.

Since main task of test case generation is to combine test factors, one can perform this task mechanically to a certain extent.

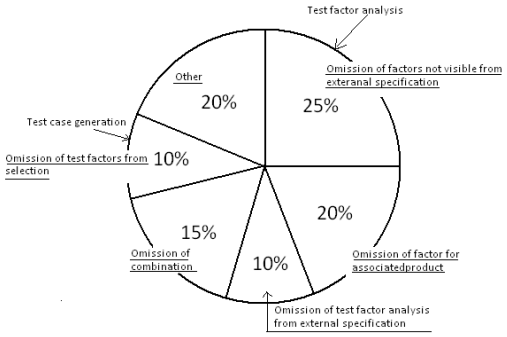

Fig.1: Reason for Failure to Detect Errors

IV. TEST FACTOR ANALYSIS

The test factor analysis process passes through the following phases:

1. Factor Analysis

A factor analysis is made by extracting input factors and environment factors from the external specification.

- Input factors

  Most of the functions of a programs run according to input explicitly supplied from outside in an instruction format, such as a command, control statement or statement. With commands, the input information is supplied in the command itself or by its operands.

- Environmental factors

  Program operations vary depending on the operating status of associated programs or hardware. These factors relating to associated programs and hardware are called environmental factors.

2. Analogy of Associated Factors

The factor analysis often begins by extracting input factors from external specifications and proceeds to identify environmental factors not explicitly covered in the external specifications; that is, the process works by gaining a clue from one keyword to next keyword.

3. State analysis

State can be analyzed in the following categories according to their type of value:

- Factor indicating numeric values
- Factor specifying a selection format
- Factor in generic name format

4. Test Factor Analysis Method

If the test factor analysis processes described above are organized into a map of test factor analysis methods, the result is shown below. [5]

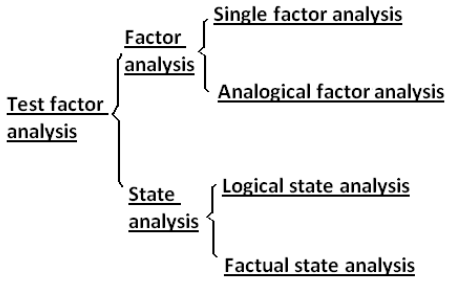

Fig. 2: Test Factor Analysis

V. PAIRWISE TESTING STRATEGY

Given the different input parameters with multiple possible values for each parameter, performing exhaustive testing which tests all possible combinations is practically impossible. Effective test cases can be made by an optimal set of tests which will effectively test the software system. Pair-wise testing is known for

its effectiveness in different types of software testing by identifying effective test factors [6 7 8].

Given a set of N independent test factors: f1, f2... fN, with each factor fi having Li possible levels: fi = {li,1... li,Li}, a set of tests R is produced. Each test in R contains N test levels, one for each test factor fi, and collectively all tests in R cover all possible pairs of test factor levels (belonging to different parameters) i.e. for each pair of factor levels li,p and lj,q, where $1 < p < Li$, $1 < q < Lj$, and $i = j$ there exists at least one test in R that contains both li,p and lj,q.

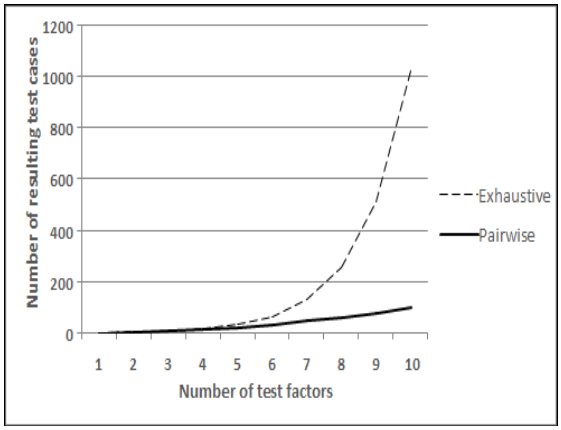

Fig. 3: Increase in number of exhaustive and pairwise tests with number of test levels

To detect interaction failures by "pairwise testing", all possible pairs of parameter values are covered by at least one test. Its effectiveness is based on the observation that software failures often involve interactions between parameters. For example, a router may be observed to fail only for a particular protocol when packet volume exceeds a certain rate, a 2-way interaction between protocol type and packet rate

However, it is very unlikely that pairwise tests would detect unusual case like combination of 3, 4 or more values; we would need to test 3-way and 4-way combinations of values. It require impractically long times to generate 3-way, 4-way, or 5-way arrays because the generation process is mathematically complex. Pairwise testing, i.e. 2-way combinations, has come to be accepted as the common approach to combinatorial testing because it is computationally tractable and reasonably effective.

VI. ALGORITHM TO INDENTIFY EFFECTIVE TEST SET

In this section, we consider the case where each parameter takes only two values. Suppose one has strings consisting of zeros and ones which all have the same length $2k$-1. Let us define the weight of a string to be the number of ones in it. Let S_{2k-1} be the collection of all binary strings of length $2k$-1 and weight k. Note that

$$|S_{2k-1}| = \binom{2K-1}{K}$$

For example, there are 10 strings of $S5$:

0 0 0 0 1 1 1 1 1 1

0 1 1 1 0 0 0 1 1 1

1 0 1 1 0 1 1 0 0 1

1 1 0 1 1 0 1 0 1 0

1 1 1 0 1 1 0 1 0 0

Pick any two strings (i.e. columns), say the first and the last. Each of these three combinations (0 1), (1 0) and (1 1) does appear at least once. Thus, if one appends a 0 at the bottom of each string of $S2k$-1, then it is possible to conclude that each of the four possible combinations (0 0), (0 1), (1 0) and (1 1) appears at least once in each pair of strings.

Algorithm:

Input: Number of parameters n.

Output: A test set.

1. Compute smallest k such that $n \leq |S_{2k-1}| = \binom{2k-1}{k}$
2. Choose any n strings from $S2k$-1.
3. Append one zero at the end of each chosen string to get a test set of size $2k$.

End Algorithm

VII. CONCLUSION

The goal of this paper is to create effective test cases for software testing. Identification of test factor is critical part of test case design. However, omission of combination of test factor combination leads to create inefficient test cases.

Using pairwise testing for identification of test factor following results can be obtained:

a. Reduction in the number of test cases
b. Detection of interaction failure

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Implementation of Hybrid Processor using FPGA

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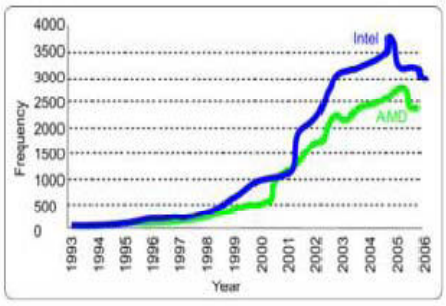
P.C.E, Nagpur

Abstract **-** Embedded and real time system designers are continually challenged to provide increased computational capabilities to meet system requirements at ever improving price/ performance ratios. Best practices are to use the commercial off the shelf (COTS) components to reduce design cost and time to market. High performance computing systems may consist of multiple multi-core processors and reconfigurable logic coprocessors. [CPU- central processing unit, COTS- commercial off the shelf components, FPGA- field programmable gate array, VHDL- very high speed integrated circuit hardware description language, HDL- hardware description language, CLB- configural logic block, IOB- input output block, EPROM- erasable programmable read only memory]

I. INTRODUCTION

An embedded system is some combination of computer hardware and software; either fixed in capability or programmable that is specifically designed for a particular kind of application device. Industrial machines, automobiles, medical equipment, cameras, as well as the more obvious cellular phone are among the myriad possible hosts of an embedded system. Embedded systems that are programmable are provided with a programming interface The clock frequencies of CPU have reached a practical limit at around 3GHz. However, higher clock frequency also means higher power consumption and processor heat dissipation. CPU manufacturers now use the improved processes to fit more and more CPU cores onto each device, each running at about the same clock frequency as their predecessors.



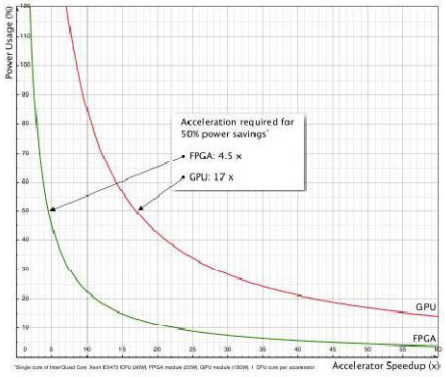
The figure above shows the graph of frequency versus year. As the year progressed, the frequencies of the two manufacturers are increased. To overcome the demand of increasing demand of clock frequency and power, a new phenomenon is being used. This phenomenon is referred as Hybrid Computing. Hybrid computing is the technique of extending a commodity with application specific instructions to accelerate application performance. The processor which depends on the functional characteristics of Hybrid Computing is referred as Hybrid Processor.

II. DESCRIPTION

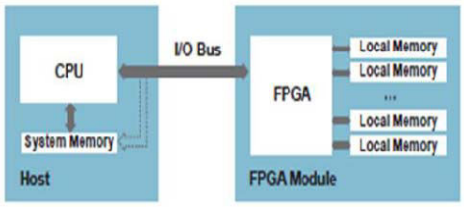
The Hybrid processor differs from conventional processor as it uses COTS components like FPGA for implementation of the parallelism and distribute the computation among several computational resources. High performance computing system may consist of multiple multi-core processors and co-processors. The use of commercial off-the shelf (COTS) components used to reduce design costs and time to market.

A hybrid model combines the advantages of both the work station server and processor pool models. This model is based on the workstation server model but with addition of pool of processors. The pool of processor may have two to eight processors for increasing speed of computation.

The implementation is on FPGA by use of Hardware Desciption Language like VHDL or Verilog. The HDL to be used dependent on the computing performance.



The above graph shows the power usage versus accelerator speedup. FPGA devices use less power than CPUs and GPUs. However for power savings, the most important factor is the attained acceleration.



The above figure shows a basic structure of Hybrid Processor. The complete computer based on the hybrid computing phenomenon is divided into two main parts, namely Host and FPGA Module. The Host part consist of the host processor, system memory and various buses. The FPGA module part consist of the processors(nearly two to eight in number), local memory and buses.

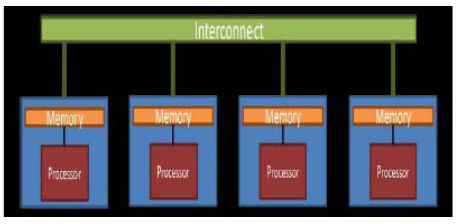
These processor is to be needed because of the increasing clock frequency of host processor. As the clock frequency is increased more power is required for delivering it. The power requirement increases the heat dissipation by the device.

III. TYPES OF PROCESSOR

The type of processor is dependent on the following two factors.

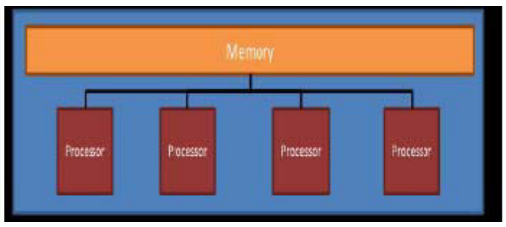
A. Depending on Memory

a) Distributed memory



The distributed memory for each hybrid processor is used. A special memory cell is designed, depending upon the number of processors.

b) Shared memory



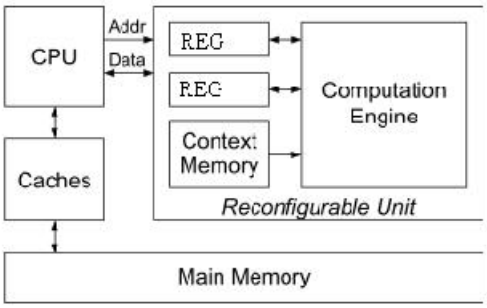
The same memory is shared by all the processors. It will reduce the size of it.

B. Depending on Clock applied

a) Synchronous: single global clock (same as the host processor). The single global clock refers to the same clock signal as the host processor.

b) Asynchronous: self clocked modules or without an input clock. The different clock is applied at the input of all modules. So, a clock circuitry for each and every module is to be designed.

IV. ARCHITECTURE OF PROCESSOR



System model outline.

The system model outline is shown in above diagram. The different blocks with their functionalities are as follows.

a) CPU: The CPU is the host processor.

b) Buses: The address and data bus is connected to the coprocessors. Buses act as an interface between the pool of processors in the reconfigurable unit (FPGA). The address bus is unidirectional whereas data bus is bidirectional.

c) Caches: It acts as an interface between high speed processor and slow memory.

d) Main memory: The main memory is the memory unit of the host processor.

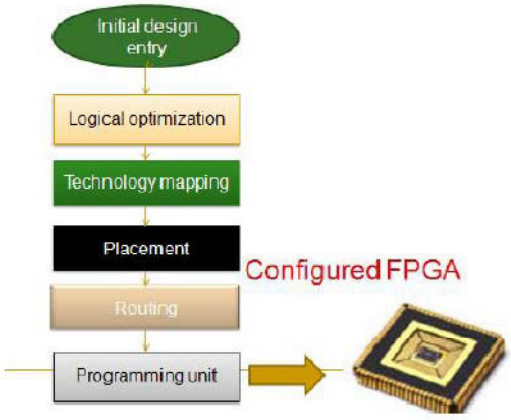
e) Registers: It consists of the two registers, which acts as a local storage in reconfigurable unit. These two registers store the operands.

f) Context memory: The context memory is the memory unit of the coprocessor, depends on the type of the hybrid processor i.e. distributed or shared.

g) Computation engine: Computation engine is the main operational unit, which can perform different operations. The result of the computation engine is stored in accumulator of host processor and depending upon that results flag gets affected.

V. DESIGN FLOW

The typical design flow of the hybrid processor is shown below.



a) DESIGN ENTRY: It provides various design entry tools like HDL (verilog & VHDL) schematics & state cad. An HDL entry is further simplified by design wizard during creation of new source and use of design templates during editing.

b) LOGIC OPTIMIZATION: It translates the HDL code into a technology independent gate-level net list. It then uses sophisticated optimization technique to minimize hardware.

c) TECHNOLOGY MAPPING: It translates the gatelevel net list to the components available in the target device, i.e., it produces a net list in terms of configural logic blocks (CLB) & I/O blocks (IOB). For FPGA targets, the synthesizer also produces a VHDL source file for post map simulation. (A cluster of 2 or 4 logic elements is called CLB, IOB are user configurable to provide an interface between external package pin & I/O logic.)

d) PLACEMENT: The software places CLBS & IOBS such that the total length of interconnections is minimized.

e) ROUTING: It allocates paths for inter CLB & inter IOB signals using the available routing resources. It also produces a VHDL source file for post routing simulation.

f) PROGRAMMING UNIT: In case of FPGA the program is first downloaded to an EPROM & transferred to FPGA on the target board during booting.

VI. OUTPUT OF SOME MODULES

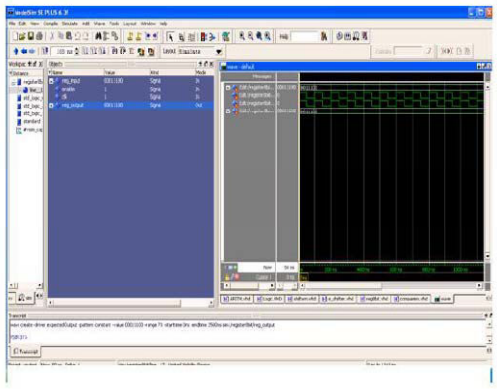


Fig. : output of 8 bit register

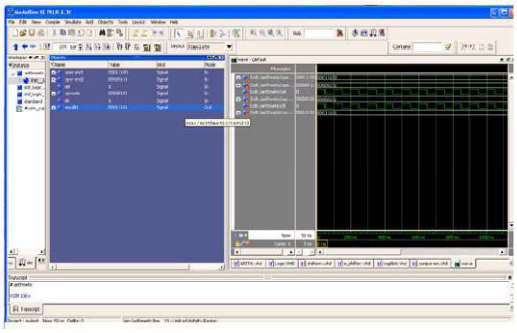


Fig. : output of Arithmetic block

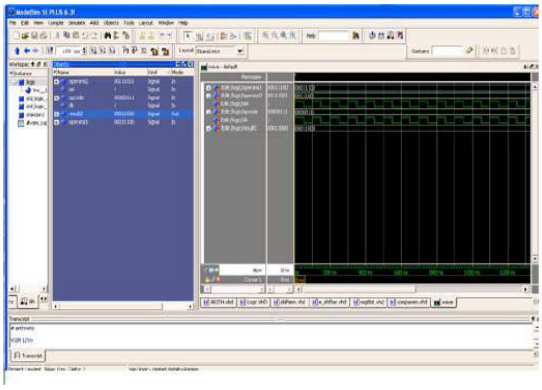


Fig. : output of Logic block

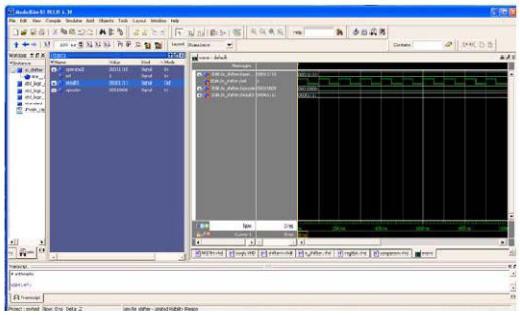


Fig. : output of Shifter

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Image Source Identification Based On Digital Single Lens Reflex Camera

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Abstract - Multimedia forensic for image source identification is based on digital single lens reflex (DSLR) camera. Digital single lens reflex (DSLR) camera has interchangeable lenses due to that imaging sensor create a persistent pattern and that pattern act as a unique fingerprint for the source identification. Multimedia Forensics has become important in the last few years. There are two main interests, namely source identification and forgery detection. Source identification focuses on identifying the source digital devices (cameras, mobile phones, camcorders, etc) using the media produced by them, while forgery detection attempts to discover evidence of tampering by assessing the authenticity of the digital media (audio clips, video clips, images, etc). In this paper, uses a novel source DSLR camera identification method based on detection and matching of dust-spot characteristics that settle in front of the imaging sensor create a persistent pattern in all captured images of camera, mobile phones, camcorders, etc. To prevent false detections, lens parameter dependent characteristics of dust spots are also taken into consideration.

Keywords: *Multimedia forensic, digital single lens reflex (DSLR), sensor dust.*

I. INTRODUCTION

Multimedia Forensics has become important in the last few years. There are two main interests, namely source identification and forgery detection. Source identification focuses on identifying the source digital devices (cameras, mobile phones, camcorders, etc) using the media produced by them, while forgery detection attempts to discover evidence of tampering by assessing the authenticity of the digital media (audio clips, video clips, images, etc). In the analog world, an image (specifically a photograph) has generally been accepted as a "proof of occurrence" of the event it depicts. In today's digital age, however, the creation and manipulation of digital images, audio and videos are made simple through digital processing tools that are easily and widely available. As a consequence, they can no longer take the authenticity of images and videos for granted, be they analog or digital. This is especially true when it comes to legal evidence. Image audio and video forensics, in this context, is concerned with uncovering some underlying fact about an image audio or video. In this paper, review several techniques in digital camera image forensics, i.e. in source camera identification and in forgery detection. Source camera identification methods explore different processing stages of the digital camera for unique characteristics and exploit the presence of 1) lens radial distortion 2) sensor imperfections, 3) color filter array (CFA) interpolation 4) inherent image features etc. Image forgery includes splicing of images to construct a new concocted image, applying region duplication/swapping to hide/relocate certain objects in the image and applying image editing to remove/add new objects from/into the image. For forgery detection, some of the methods inspect the image for inconsistencies in chromatic aberration, lighting, and camera response function (CRF) as signs of forgery. Others try to detect certain modes of manipulation using JPEG quantization tables, bicoheren and robust matching.

A. Digital single lens reflex (DSLR)

This paper uses a novel source camera identification method based on detection and matching of dust-spot characteristics that settle in front of the imaging sensor create a persistent pattern in all captured images of Digital Single Lens Reflex (DSLR) camera. In this paper DSLR camera is use because it has unique features like sensor dust pattern than other cameras. It is used in high profile function, larger and higher quality sensors, low noise power, parallex-free optical viewfinder that allows error free viewing of the scenery, less shutter lag, interchangeable lenses, and better control over depth of field.

DSLR cameras showed a consistent growth with a total market and a 59% increase from the 2009figure. Not surprisingly, DSLR cameras also take the top place in most popular camera lists of photo sharing websites like and social networking like facebook. For instance, the top five cameras for November 2010 in Flickr

(flickr.com) and Pbase (pbase.com) photo sharing websites are all DSLR cameras. Unlike the compact camera market which is cluttered with various brands like Sony Olympus, Canon, Nikon have over 95% market share in DSLR market in India of which Nikon claims to have 55% market share.

In Section II, we investigate the optical characteristics of sensor dust as a function of imaging parameters .In section III, a model-based dust spot detection method and its use in source camera identification.Section IV and V are presented by conclusion and references

B. Related work

Choi et al [11] propose the lens radial distortion as a fingerprint to identify source camera. Radial distortion causes straight lines to appear as curved lines on the output images and it occurs when the transverse magnification MT (ratio of the image distance to the object distance) is not a constant but a function of the off-axis image distance r.
Although this method is not tested for two cameras of the same model, based on the authors' arguments on radial distortion differences, they can expect a low accuracy. Additionally, this method will fail to measure radial distortion if there is no straight line in the image since the distortion is measured using the straight line method.

Geradts et al [1] examine the defects of CCD pixels and use them to match target images to source digital camera. Pixel defects include point defects, hot point defects, dead pixel, pixel traps, and cluster defects. To find the defect pixels, a couple of images with black background are taken by each of the 12 cameras tested and compared to count the common defect points that appear as white. The result shows that each camera has distinct pattern of defect pixels. Furthermore, for cameras with high-end CCD, the authors cannot find any visible defect pixel, which means that not all cameras necessarily have pixel defects. In addition, most cameras have built-in mechanisms to compensate for the defective pixels. Therefore, the method cannot be directly applied for all digital cameras.

Identifying source camera based on sensor pattern noise is proposed by Lukas et al [10].The pixel non-uniformity (PNU), where different pixels have different light sensitivities due to imperfections in sensor manufacturing processes, is a major source of pattern noise. This makes PNU a natural feature for uniquely identifying sensors. The study 9 camera models where 2 of them have similar CCD and 2 are exactly the same model. The camera identification is 100% accurate even for cameras of the same model.

The result is also good for identifying compressed images. One problem with the conducted experiments is that the authors use the same image set to calculate both the camera reference pattern and the correlations for the images. It run several experiments with this model for cropped images. It turns out that the model fails to predict the source camera of cropped images.

Bayram et al [8] explores the CFA interpolation process to determine the correlation structure present in each color band which can be used for image classification. The main assumption is that the interpolation algorithm and the design of the CFA filter pattern of each manufacturer (or even each camera model) are somewhat different from others, which will result in distinguishable correlation structures in the captured images. No experiment is run for cameras of the same model but we expect the method to fail because cameras of the same model normally share the same CFA filter pattern and interpolation algorithm. In addition, the authors have pointed out that this method does not work well for compressed images.

Kharrazi et al [3] identify a set of image features that can be used to uniquely classify a camera model. The 34 proposed features are categorized into 3 groups: Color Features, Image Quality Metrics, and Wavelet Domain Statistics. Features are extracted from images of two cameras, which are then used to train and test the classifier. The result is as high as 98.73% for uncompressed images and 93.42% for JPEG images compressed with a quality factor of 75. The accuracy rate drops to 88% when five cameras are used. Hence, this method does not work well for cameras with similar CCD and is unsuitable for identifying source cameras of the same model. Furthermore, it requires all cameras to take images of the same content and resolution, which is not easy in practice.

II. CHARACTERISTICS OF SENSOR DUST:

A. Intensity degradation due to dust spot:

Essentially, dust spots are the shadows of the dust particles in front of the imaging sensor. The shape and darkness of the dust spots are determined primarily by the following factors: distance between the dust particle and imaging sensor, camera focal length, and size of aperture. A general optical model showing the formation of dust spots is given in Fig. 3. When the focal plane is illuminated uniformly, all imaging sensors will yield the same intensity values. However, in the presence of sensor dust, light beams interact with the dust particles and some of the light energy is absorbed by the dust particles. The amount of the absorbed energy is directly related to the parameter -number (F/#) which is defined as the ratio between the focal length f and aperture A

$$f\text{-number} = \frac{f}{A}. \qquad (1)$$

At small apertures and high f-numbers, the light source can be assumed to be a pinpoint source resulting in a relatively narrow light cone which can be blocked mostly with a tiny sensor dust. As a result, a strong dust shadow will appear on the image. This phenomenon is illustrated in Fig.1. On the other hand, for wide apertures or small f -numbers which cause wide light cones in the DSLR body, most light beams pass around the dust spots causing a blurry and soft blemish in the image. In Fig.2 the actual intensity degradations caused by dust spots are shown for different -numbers. It can be seen from the figures that the change in -number affects the intensity and radius of the dust spot wherein an increase in the f –number (smaller aperture) causes dust spots to appear darker and smaller.

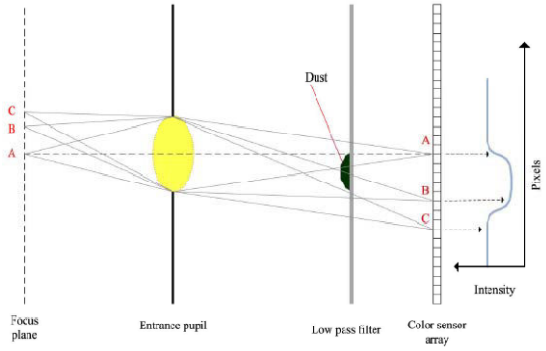

Fig1. Formation of Dust Spot under uniform illumination

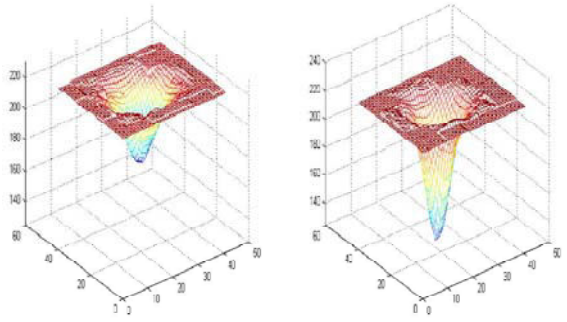

Fig.2. Intensity degradation due to the dust spot.

B. Dust-Spot Shape:

The dust particles in front of the imaging sensor mostly appear as round-shaped blemishes. However, dust spots with different shapes are also possible due to larger particles, such as lint or hair (Fig.3).

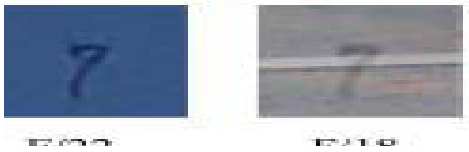

Fig.3. Spot of hair/lint for different f -numbers (Nikon D40).

Since these large spots, with unique shapes, are likely to cause very large intensity degradations, they are easily noticeable. Although this type of sensor dust is very suitable for camera identification, it is likely to attract the user's attention due to their annoying appearance. As a result, they are more likely to be cleaned out. Therefore, in this project, we have focus on dust spots due to much smaller particles that yield round-shaped dust spots that are less likely to be cleaned by many users and are, in fact, difficult to clean as discussed earlier.

C. Dust-Spot Size:

The formation of dust spots as a function of the camera parameters is analyzed.

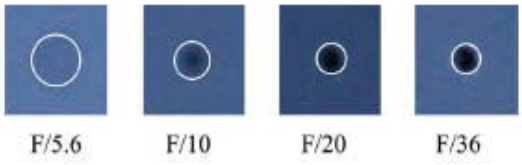

Fig. 4. Same dust spot for different f –numbers

Fig.4 shows the change in diameter of a dust spot for fixed focal length and different apertures. It can also be seen from the table that the dust-spot size decreases with a decrease in aperture.

F-number	5.6	10	20	36
aperture	9.82	5.5	2.75	1.53
Max-intensity degradation	11	46	61	83
Dust-spot diameter[pixels]	20	14	11	10

Table II. Dust-Spot properties for different –f-numbers (f = 55 mm)

III. FORENSIC USE OF SENSOR DUST

In this section, we develop a technique for camera identification based on sensor dust detection. The use of dust spots for Source camera identification first requires determining the positions of dust spots in an image.

Since dust particles do not tend to move easily, they appear in all images taken with high f-numbers, and their proper cleaning is not trivial, these dust-spot locations can be used as a unique fingerprint of a DSLR camera. This fingerprint can be represented by a camera dust template that includes information on all detectable dust spots. It must be noted that this template can be directly obtained from images taken by the camera at a high f-number setting or from a number of images when the camera is not available by collating dust spots detected from different images together. To decide whether an image is taken by a given DSLR, the dust spots detected in an image can be compared to those in the camera dust template and a decision is made depending on the match between detected dust spots and the template.

A. Detection of Dust spot

We propose a model-based dust detection scheme that utilizes dust-spot intensity and shape characteristics in detecting dust spots. In our proposed detection scheme, we model dust spots based on their two major characteristics: A) an abrupt change on image intensity surface as a function of the f-number and B) they appear mostly in the form of rounded shapes. As mentioned before, sensor dust can be viewed as black, out-out-focus spots with a soft intensity transition. Our observations of various actual dust spots also confirm that they have Gaussian-like intensity degradations. This phenomenon can be viewed in Fig.2. Inspired from these figures and many other examples, we utilize a Gaussian intensity loss model (i.e., a 2-D Gaussian function to model dust spots). Our model for the dust spot is expressed as follows:

$$\text{intensity loss}(x,y) = \frac{-G}{\sqrt{2\pi\sigma^2}} \cdot e^{-(x-w)^2+(w-y)^2/2\sigma^2}$$
$$x, y = 0, \ldots, 2w$$

Where G– Gain factor, σ - Standard deviation, w – template width

Essentially, dust-spot dimensions depend on the f – number and dust size. To capture this relation in our model, is selected to adjust the size of the dust-spot model. The intensity loss of the model is controlled by the parameter Although, for a given image, the f-number can be obtained From the EXIF data, the actual dust size cannot be known. In detecting dust spots in an image, we correlate the Gaussian dust model with the image for various values over all pixel positions via fast normalized cross correlation (NCC) [12]. This results in a 2-D map of values where each value is computed by cross-correlating the Gaussian dust model with a window of size 2w×2w sliding over the image, which will be referred to as NCC output.

In the NCC output, values higher than an empirically set threshold are selected as potential dust-spot candidates. To reduce the search range of the parameter and to speed up the detection process, all images are suitably down sampled to a mid resolution (800 ×533) while preserving their aspect ratio.

Our measurements in Table III indicate that dust spots generally have an area that is less than that of a window of 10 ×10 pixels. Based on this observation, we chose or which correspond to small (6×6 pixels) and large (12 ×12 pixels) dust spots, respectively. To exemplify the relation between the NCC output and model parameter , our dust detection scheme was applied to various dust spots. In Table IV, NCC local maxima values computed through our detection scheme for different dust spots taken from various DSLR cameras (2 ×2 pixels to 20 ×20 pixels) are given. As seen from the table, the corresponding NCC local maxima of dust spots takes values between 0.44 and 0.81 which are sufficiently high for dust-spot detection. To visualize the spatial NCC output variations, NCC mesh plots of two different dust spots are given in Fig. 5. In the figure, our dust model produces Gaussian-like NCC outputs with high NCC value sat the centre of dust spots (0.81 for small dust and 0.53 for are latively large one). In the camera identification phase, the proposed dust-spot detection scheme is repeated for each value (i.e.,$\sigma = 1,2$). Then, all detected dust-spot positions are combined together to detect various-sized dust spots in a given image.

TABLE III
MAX. DETECTED DUST-SPOT SIZE FOR DIFFERENT DSLR CAMERAS (IMAGE SIZES: 800 × 533)

DSLR camera	Max. dust spot size [pixels]	f-number
Sigma SD10	3×3	11
Sigma SD9	5×7	5.6
Nikon D1	7×7	N/A
Nikon D50	8×8	10
Nikon D70	7×7	N/A
Canon EOS Rebel	7×8	22
Canon EOS Rebel XTi	9×9	13

TABLE IV
MAX. NORM. CROSS-CORRELATION (NCC) OUTPUTS FOR VARIOUS DUST-SPOT (IMAGE SIZES: 800 × 533)

Dust no	Dust spot size [pixels]	Max depth	Max NCC (G=5, 2w=20+3σ)
1	2×2	13	0.71 ($\sigma = 1$)
2	6×6	33	0.81 ($\sigma = 1$)
3	14×14	9	0.53 ($\sigma = 2$)
4	20×20	11	0.44 ($\sigma = 2$)

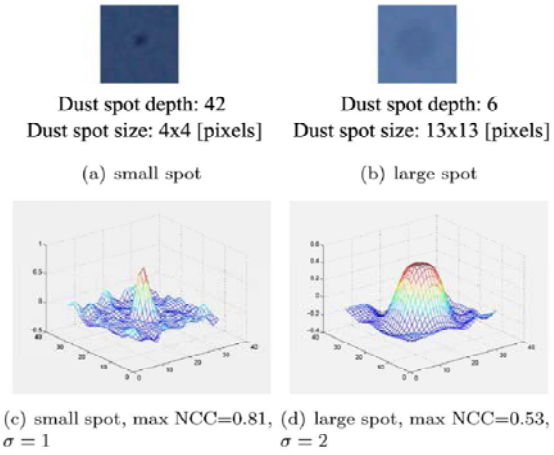

Fig. 5. Normalized cross-correlation (NCC) outputs for different dust spots.

4×4 [pixels] dust (left), 13×13 [pixels] dust (right).

A. Camera Dust Pattern Generation

Digital Camera Available

In this case the dust pattern of an image can be generated by Taking the picture of distant smoothly varying scenery by manually setting the focal length to high values (f/32 or f/36).Then proposed dust detection method is applied to create dust pattern of the camera.

Images Acquired with The DSLR Camera are Available

When the camera is not available but rather a number of images taken by the camera is present, the dust points that are determined by correlation and through shape characteristics in each image is superimposed together to form the dust pattern/template of the camera. Once the template is created, a threshold is applied to the template to reduce the number of falsely labelled specks in the dust pattern. The underlying idea of applying a threshold to the template is that the actual dust specks should show up at least in two or more images. Since the probability of getting a false dust candidate at the same position in multiple images is very low, we expect that false positives due to image content will be eliminated after thresholding.

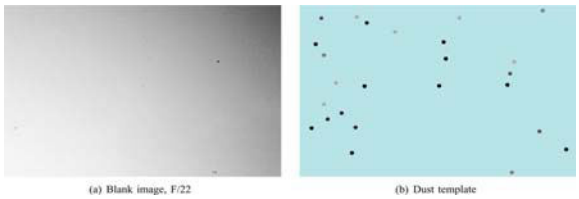

Fig. 6. Canon EOS dust template created with three blank images with different f -numbers (F/13, F/22, F36).

The dust candidates which have higher confidence values than a fixed threshold are considered to represent the dust pattern of the camera.

C) Camera Identification*:*

The final step of DSLR camera identification is done by matching the dust spots detected in an image with dust spots in the camera dust template. The identification process is comprised of three steps:

Step 1) dust-spot detection and matching;

Step 2) computing a confidence value for each matching dust

Step 3) decision making.

In the first step, dust spots are detected as explained in Section III-A. Once dust spots are located, each dust position is matched with the dust positions in the camera dust template. The comparison is realized by measuring Euclidian distances. If the distance is lower than a predetermined value, the corresponding dust position is added to the matching dust-spot list. In the second step, three metrics are computed for each of the matching dust spots as follows.

1) The dust occurrence metric m1 is the number of coinciding dust for the corresponding dust spot in the dust template. Higher values of correspond to salient dust spots.

2) Smoothness metric m2 presents the smoothness of the region in which a dust spot was detected. Measuring the amount of local intensity variations is essential in making decisions since dust spot detection in smooth regions is more reliable than in busy regions. This is computed via the intensity gradient around the dust spot as a binary value. For a smooth region, becomes one, and for a nonflat or nonsmooth region m2 around the dust spot, it becomes zero.

3) Shift validity metric m3 indicates the validity of a dust spot based on the shift it exhibits. To compute , we do the a Each dust spot in the matched dust-spot list is tracked in all template images, used in template generation. (It should be noted a different subset of dust spots will be detected in each image.)

b) For each dust spot in the list, a set of the shift vectors (i.e., magnitude and angle) is computed by measuring the shifts between a dust spot and its matched counterparts in the template images).

c) Shift vectors associated with each of the template images are collected together.

IV. CONCLUSIONS

In this paper, we have introduced a latest technique of Multimedia forensic in that we have concentrated on source DSLR camera identification scheme based on sensor dust traces. The location and shape of dust specks in front of the imaging sensor and their persistence make dust spots a useful fingerprint for DSLR cameras. Although many DSLR cameras come with built-in dust removal mechanisms, these hardware-based removal solutions are not as effective as they claim to be. Besides, since most dust spots are not visible or visibly irritating, most DSLR users ignore them completely. To the our best knowledge, this is the first work in the literature which uses sensor dust spots for individual camera identification.

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Electronic Power Assisted Steering System

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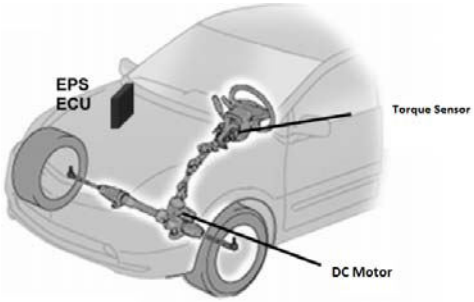
Abstract - Electric power steering offers greater vehicle safety by adapting variable steering ratios to human needs, filtering drive train influences and even adjusting active steering torque in critical situations. In addition, it can make cars lighter and more fuel efficient when compared to those using hydraulic steering systems.

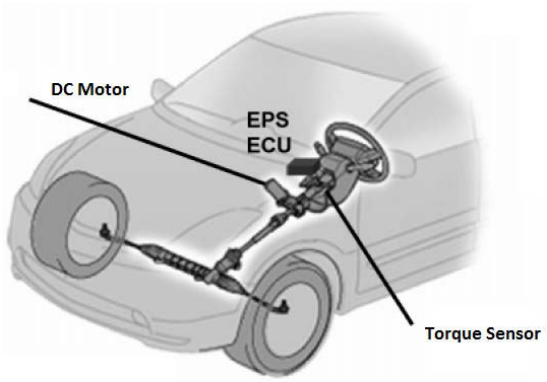
The central electronic elements of today's power steering systems are modern 32-bit microcontrollers, ARM controllers (MCUs). Only high-performance MCUs can provide sufficient computing power and specialized peripherals for complex motor control functions. Since power steering is a safety-critical function, it also requires new MCU elements that support the functional safety of the overall system.

Keywords – *EPS- Electronic Power Steering System, ECU- Electronic Control Unit*

I. INTRODUCTION

The central electronic elements of today's power steering systems are modern 32-bit microcontrollers, ARM controllers (MCUs). Only high-performance MCUs can provide sufficient computing power and specialized peripherals for complex motor control functions. Since power steering is a safety-critical function, it also requires new MCU elements that support the functional safety of the overall system the central electronic elements of today's power steering systems are modern 32-bit microcontrollers (MCUs). Only high-performance MCUs can provide sufficient computing power and specialized peripherals for complex motor control functions. Since power steering is a safety-critical function, it also requires new MCU elements that support the functional safety of the overall system.





Steering Mechanism

The topic discusses the steering control mechanism and components involved in it.

Steering Gear

Turning the steering wheel transmits the torque to the pinion, which causes input shaft to rotate. The input shaft and pinion bar are linked through torsion bar, which twists until torque and reaction force are equal. The twist in the torsion bar is detected by torque sensor which converts the applied torque into electrical signals.

DC Motor

A worm gear assembly is used in combination with DC motor to transmit the torque to column shaft.

Reduction Mechanism

Reduction mechanism transfers the motor power assist to the pinion shaft. It consists of ring gear that is connected to pinion shaft and pinion gear which is in turn integrated with motor shaft.

Torque Sensor

It determines the amount of torque applied to the steering and converts it to electrical signal. EPS ECU uses this signal to determine the amount of power assist the motor should provide.

EPS CPU

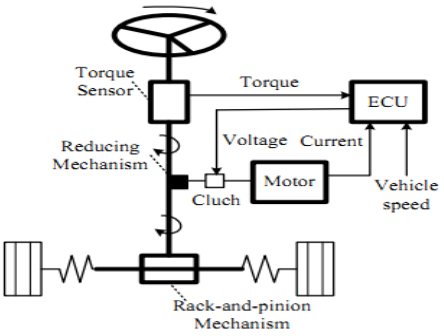
It receives signals from various sensors and determines the assist current to be applied to the DC Motor on the basis of current vehicle condition.

Malfunction Detection

It is one of the tasks performed by the EPS CPU, by detecting malfunction and alerting the driver by warning light.

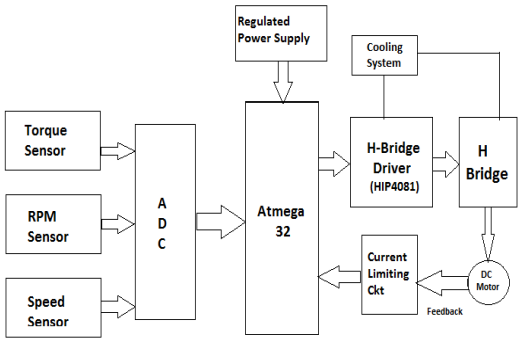
II. BASIC PRINCIPLE OF EPS

Compared with the traditional hydraulic steering system (HPS), Electric Power Steering (EPS) system adopts motor to offer the driver assistance directly and has the advantages of economy, handiness, easy adjustment, less noise and waste oil pollution and so on the composition and working principle of EPS system . EPS system is mainly composed of speed sensors, steering wheel rotation sensors (including torque sensor and speed sensor), electronic control unit (ECU), power drive circuit, clutch, DC motor and so on. ECU decides the rotational direction and suitable assistant torque of motor according to the sensors' output signals, sending control signals to motor and clutch, and then controlling motor's rotation through power drive circuit. The output of motor from the decelerating gearbox drives rack-and-pinion mechanism to produce the corresponding steering power. The magnitude of the motor torque can be changed arbitrarily by control algorithms to offer the necessary transmission power value to transmission mechanism.



III. ELECTRONIC CONTROL UNIT (ECU) DESIGN

EPS ECU consists of microcontrollers A/D convertors, motor drive circuitry (H-Bridge and n-channel mosfet Drive) and regulated power supply with force cooling system. Following diagram makes it clear.



The three analog information obtained from the three sensors are converted using an adc an ATMEGA-32 microcontroller is used to process the data obtained from adc,

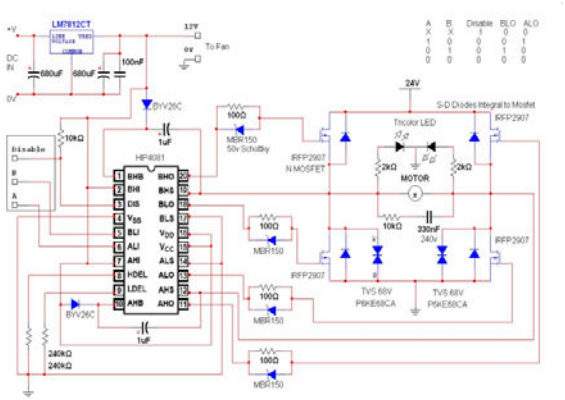
ALGORITHM used to drive the ESP

1. When the output of RMP sensor is at high level then EPS is enabled and if low it is disabled.
2. When speed of the vechicle determined by speed sensor exceeds 40km/hr EPS turns off and the steering is derived by mechanical assistance.
3. When the voltage ratings of the Torque sensor is 2.5v then PWM=0, when Torque sensors voltage>2.5 the wheels are rotated in right direction.

Torque sensors voltage<2.5 the wheels are rotated in left direction.

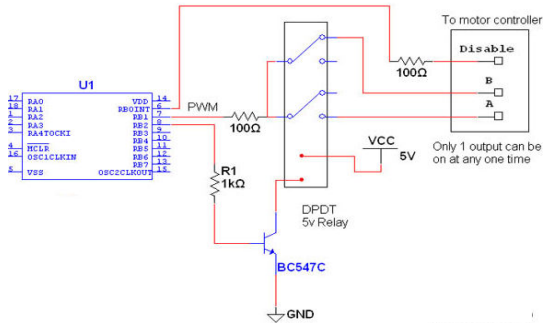
4. when the current ratings of current limiting circuit exceeds 51Amps ,output of this circuit becomes high and H-brisge is disabled.

Here the H bridge consist of 4 N channel mosfets IRF3205 having current ratings of 110 Amps. It requires a mosfet driver which we have used is HIP4081 its circuit diagram can be shown by following diagram.



The schematic is fairly self explanatory in the way of parts and values. If we need higher current abilities, simply parallel 2 or 3 Mosfets together on each leg of the H Bridge. Just don't add too many as you increase the Gate charge and hence power required turning the Mosfets on. We may also need to up-rate the Transient Voltage Suppressors (TVS) to more than 68V.

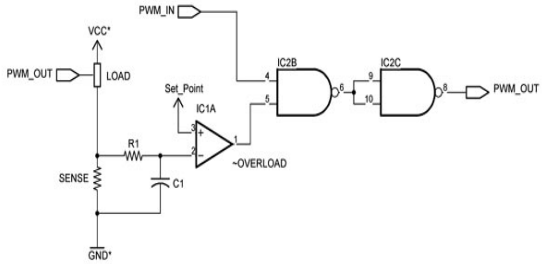
Simply connect the A, B and Disable lines to your chosen microcontroller, or even switches if you don't want variable speed control. The HIP will accept 5v Logic. By using a microcontroller, you can send a PWM signal to either the A or B inputs to make the motor spin forward or back at any speed desired. Make both inputs low to enter brake mode. The disable pin is an active low and makes all outputs enabled.



We must make sure that A and B are never on at the same time. For a failsafe, you can use a relay in-between your micro and the HIP to switch the PWM signal to either A or B. This has some big advantages in that you only need 1 PWM output from your micro and only 1 input can be on at any one time. Simply toggle the relay with your micro and a transistor. This is the method I we use.

Current Limiting

The output of a current sensor could be fed to one side of a comparator, with the other side being set by a fixed (or variable) voltage reference. When the current draw rises above acceptable limits, the comparator's output can be used to turn off the circuit



Power and heat:

The power that the MOSFET will have to contend with is one of the major deciding factors. The power dissipated in a MOSFET is the voltage across it times the current going through it. Even though it is switching large amounts of power, this should be fairly small because either the voltage across it is very small (switch is closed - MOSFET is on), or the current going through it is very small (switch is open - MOSFET is off). The voltage across the MOSFET when it is on will be the resistance of the MOSFET, Rds (on) times the current going through it. This resistance, RDSon, for good power MOSFETs will be less than 0.02 Ohms. Then the power dissipated in the MOSFET is:

$$P = i_a{}^2 R_{DSOn}$$

For a current of 40 Amps, RDSon of 0.02 Ohms, this power is 32 Watts. Without a heat sink, t he MOSFET would burn out dissipating this much power. Choosing a heat sink is a subject in itself.

The on-resistance isn't the only cause of power dissipation in the MOSFET. Another source occurs when the MOSFET is switching between states. For a short period of time, the MOSFET is half on and half off. Using the same example figures as above, the

current may be at half value, 20 Amps, and the voltage may be at half value, 6 Volts at the same time.

Now the power dissipated is 20 × 6 = 120 Watts. However, the MOSFET is only dissipating this for the short period of time that the MOSFET is switching between states. The average power dissipation caused by this is therefore a lot less, and depends on the relative times that the MOSFET is switching and not switching. The average dissipation is given by the equation.

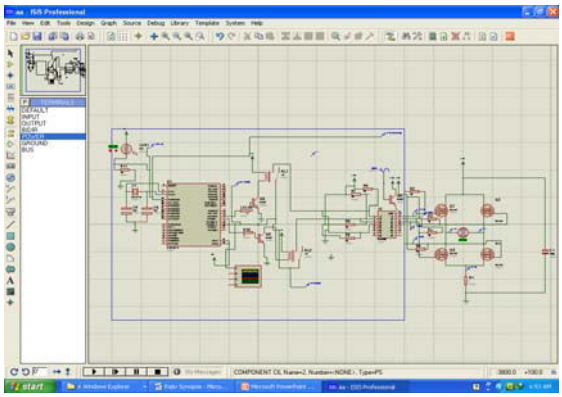
$$480W \times \frac{time\_to\_switch\_over}{time\_between\_switchings}$$

The algorithm for the circuit

- The values that is the value in analog format is obtained from the non contact hall effect sensor and the 10 bit adc of the atmega 16 accepts the value, the value ranges from 0.8-2.5-4.2
- The controller after sensing the value from adc port produces an pwm wave
- The condition is such that the value of pwm is maxmum at the two extremes 4.2 and 0.8
- The value of pwm is 0 i.e. the value when obtained as 2.5 it corresponds to zero pwm
- This pwm signalis activated and the pord d0 and d1 of the controller is used to switch the relay on
- When one port is on the relay will be on to provide an appropriate pwm according to the value obtained from adc ie port pin d5
- This pwm signal is given to the pin of hip which switches the two mosfets on and off according to the requirement.

Heat sinks are used for extra protection of the mosfets, a fan is also used inorder to provide a forced cooling to the entire system.

Proteus simulation for the circuit



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Design and Evaluation of Smart Technology Innovative Wearable Displays

(Acceptability and Objection Aspects)

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Abstract - To fullfill the promise of virtual reality, display devices need to be independent, so that you don't have to be tethered a computer, tablet or phone.They should allow natural interaction so that you can use them without reaching for an external input device and should provide access to your content and applications.Traditional interaction devices such as computer mice do not adapt very well to immersive environments, since they were not necessarily designed for users who may be standing or in movement.The objective of this work is to study how to adapt smart technology from touch surface based systems to 3D virtual environments to reduce this physical rupture from the fully immersive mode.The paper also describes smart goggles technology and its applications in various fields.In order to do this, conceptual and experimental studies have been performed on Natalia 3D goggles incorporating smart goggles technology.

Keywords - *3D User Interaction, Virtual Reality, Personal Computer, Smart Goggles, Augmented Reality.*

I. INTRODUCTION

"The ability to use interactive goggles without wires and without the need for an external computer opens up new opportunities for applications that benefit from limitless tracking area, greater portability, and on-board intelligence.''

Virtual Reality (VR), is a term that applies to computer-simulated environments that can simulate physical presence in places in the real world, as well as in imaginary worlds. The simulated environment can be similar to the real world in order to create a lifelike experience —for example, in simulations for pilot or combat training—or it can differ significantly from reality, such as in VR games. In practice, it is currently very difficult to create a high-fidelity virtual reality experience, due largely to technical limitations on processing power, image resolution, and communication bandwidth; however, the technology's proponents hope that such limitations will be overcome as processor, imaging, and data communication technologies become more powerful and cost-effective over time[1].

In recent years, several research initiatives in the field of VR have focused on the development of interaction techniques for the selection and manipulation of objects, navigation and way finding[2][3][4]. Since interface controls are an important part of conventional desktop interfaces, adapting these controls for virtual environments is necessary. A limited number of control widgets, like buttons, can be easily accessed, but that alone does not adequately suffice for more complex situations such as selection, menu navigation, and alphanumeric input. Thus, all solutions that enable 2D menus adapted to immersive environments face the problem of effectively reaching a menu item in the interaction space [5].

Some devices were created specifically for immersive environments, the user is forced to make several changes of context every time it is necessary to accomplish a task which is not supported in immersive mode. These constant changes in the context of immersion signify a break in the way a user interacts with the application. When considering the current advances achieved by interfaces based on single or multi-touch gestures, it was realized that there is a potential to use such concepts in immersive virtual environments. The literature presents many initiatives towards introducing mobile devices as interaction devices in virtual environments [6][7]. This is mainly due to the fact that modern mobile devices generally have these modern interface resources integrated and smart phones and tablets are considered quite simple and useful for gesture interactions. However, they still require the user to hold the device when interacting with the immersive environment.

Based on these ideas, the aim of this paper is to explore the possibilities of using a touch-like interface in an immersive virtual reality environment using a virtual touch screen mapped in the 3D space. Smart Goggles are a new type of virtual reality goggles.

Smart Goggles are to goggles that smart phones are to phones. By adding a CPU, an operating system and the ability to install applications, smart phones became much more than just phones. By adding a touch screen, smart phones made it easy to interact with these new features and applications. They follow the same route. By adding a powerful CPU, initially running Android, Smart Goggles can run numerous applications right on the goggles. By adding the unique ability to monitor hand movements, Smart Goggles add a powerful way to interface with the goggles. At the same time, they are still goggles: they have a 3D display, wide field of view, head tracker and more. The remainder of this paper is organized as follows. Section II describes the technology introduced with its design and operating modes. A proposed smart technology based product is introduced in section III. Its applications in section IV and challenges in section V. Section VI presents the conclusions and future work proposals are described in section VII.

II. SMART GOGGLES TECHNOLOGY

Smart Goggles technology can be well defined as *'system on a module'* technology. This technology powers new types of gaming and entertainment goggles that are mobile and feature real-time, 360-degree tracking of the hands from the user's perspective, adding intelligence, natural interaction, and true portability to goggle designs. The biggest differentiating feature of the these goggles is that they're fitted with an actual on-board computer which contains a dual core chip with a 3D graphics co-processor.

Smart Goggles is an underlying architecture and technology. It allows building a new generation of 3D gaming and entertainment platforms. Think about this technology as you would think about a brand new quad-core processor. Yes, the processor has a price, but the processor itself is not enough to run a game – you need to build a system around it. Fortunately, these goggles makes building 3D, immersive systems faster and easier, but by itself can't run a game but when this technology is licensed with different products can take different shapes and features: a fully-immersive product for the ultimate 3D gaming and entertainment; a see-through model that allows true augmented reality applications; a co-processor for a tablet that extends its power and applications to 3D and natural interaction and more and more.

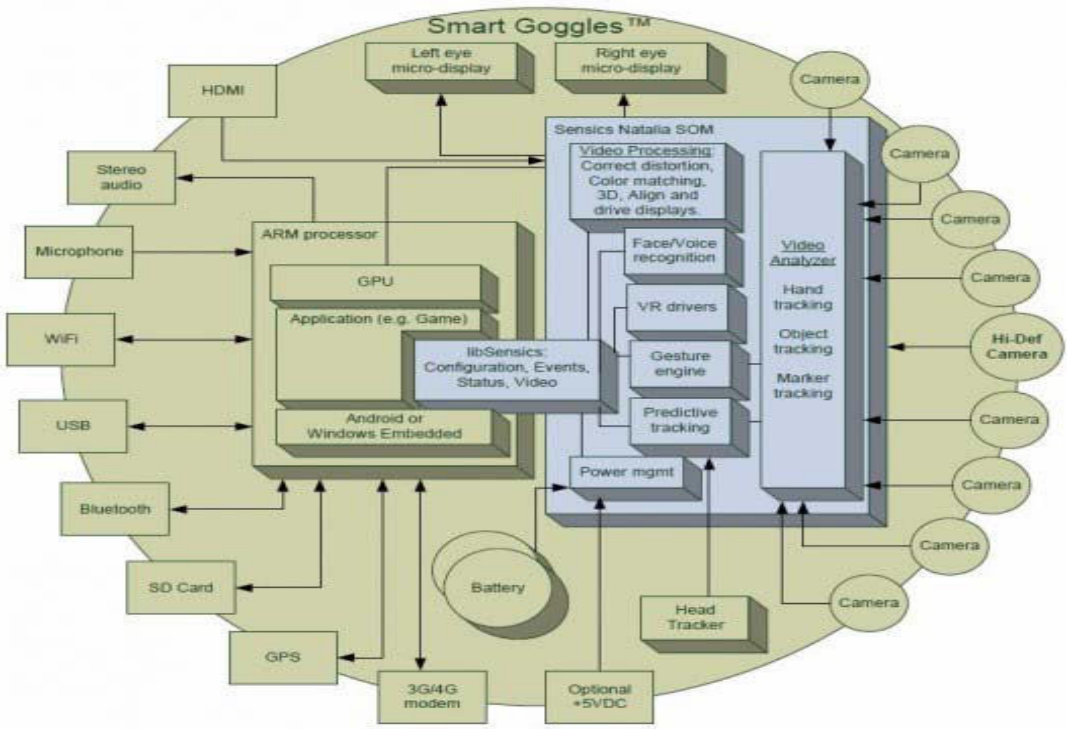

Fig. 1: Smart Goggles Block Diagram

.Smart Goggles typically include the following components:

- A powerful application processor, typically running Android or Windows Embedded, allowing you to download, run and store applications locally – on the goggles – and take them with you.
- A unique system for first-person hand tracking, providing natural interaction with the applications. By using hand tracking data – provided through the libSensics software library, application developers can use the hands to interact with 3D content, to play a 360 degree 3D game and to provide on-board user interface.
- A virtual reality engine that provides almost everything you need to build goggles: display drivers, predictive head tracking, video processing, communications and more.

Block diagram of smart goggles is shown in figure 1.

2 .1. Architectural components

The key architectural components are described below, grouped into key functions

2. 1.1). Natural interaction

The natural interaction subsystem is responsible for providing both raw and processed data to the application. Data includes:

- Head tracking information, including data processed through a predictive tracker algorithm. Raw data is typically read from a 6 sensor or 9-sensor tracker. Different tracker architectures are supported. Data includes angular position (yaw/pitch/roll), velocity and acceleration, as well as linear (x/y/z) position, velocity and acceleration.
- Hand, object and marker tracking information. High-speed hardware analyzes signals coming from multiple cameras to detect and locate hands as viewed from the user's perspective. The exact instantaneous tracking area is determined by the number and placement of the cameras, as well as their particular specifications. Since the tracking moves with the user, tracking area is limitless. The raw data includes X,Y,Z location and orientation as seen from the user's viewpoint. This data is also be processed through predictive tracking algorithms.
- Combined data: by combining both head and hand tracking information, hand and object location are also be provided in the world coordinate system.
- Gesture analysis. A gesture engine combines head and hand data to detect and report gestures which drive user interface.

2.1.2).Video management

The video management subsystem is responsible for real-time video processing that is required for optimal display on the specific micro-displays and optics selected for the goggles. This includes:

- Detection of video resolutions.
- Scaling of incoming video to fit displays.
- Processing of side-by-side video signals to make them suitable for stereo viewing.
- Color matching between displays.
- Contrast, brightness and gamma controls.
- Distortion correction to allow lower-cost optics to be used while still producing high-quality results.
- Electrical driving of the actual micro displays
- Noise reduction

The reference design includes dual SXGA OLED displays and optics with a diagonal field of view of 65 degrees.

2. 1. 3).Application processor

The application processor executes the following:

- An operating system. In the reference design, this is an Android 4.0 build, but other versions of Android or other operating systems such as Windows Embedded are supported.
- libSensics - an application library that manages the various hardware components and provides application developers with full access to their capabilities
- If required, application-specific software such as voice or face recognition
- The actual application: a game, a simulator, a media player, etc.

2. 1. 4). Power management

They are designed to be portable and thus battery-operated. While several power management schemes are possible, the reference design includes a pair of rechargeable batteries that can be recharged inside or outside the goggles. A hot swap capability allows replacing one battery while the unit continues to be powered from the other.

2. 1.5).Connectivity and expansion

They are designed to be expandable and to be connected to the outside world. This is why the reference design includes:

- WiFi for connecting to networks such as the Internet or to other devices

- Bluetooth for local peripherals or to be paired with phones and tablets
- Accessible SD card
- External HDMI input for those instances where video comes from outside the goggles
- High-definition cameras to support augmented reality, face recognition and more
- and more…

2. 2.Operating Modes

Smart Goggles can be used in multiple modes. Here are some examples:

2. 2.1).Standalone

A standalone runs the application locally on the goggles. These applications can access the Internet, and can use the head and hand tracker in a goggle for natural interaction and a fully immersive experience. A typical design might include a dual-core ARM processor with a 3D accelerator, allowing high-quality graphics in an ultra-portable package.

2. 2. 2).Connected to a phone or tablet

When running these goggles connected to a phone or a tablet, several opportunities present themselves, such as:

- The application can run on the goggles or on the phone. Alternatively, the application could be distributed: graphics and real time interaction on the goggles. Some user interface on the phone and some on goggles.
- The application could use connectivity options from either the goggles or the phone.
- Existing content or applications from the phone/tablet could be displayed on the goggles for maximum impact.
- Head and hand tracking information can be relayed to the phone or tablet via a Bluetooth, WiFi or wired connection.

2.2.3). Connected to a PC or game console

When connected to a game console or PC, these can serve as both the display device as well as the user interface device, whereas the PC or game console could use existing content and high-quality graphics processing units to render scenes. The video from the PC or game console can be sent via a standard wire or via a low-latency wireless video link to the goggles. Head and hand tracking information can be relayed to the phone or tablet via a Bluetooth, WiFi or wired connection.

III. NATALIA IMMERSIVE 3D GOGGLES

In order to realize the potential of smart goggles, Sensics, a Columbia, Maryland, company, developed a complete product based on this technology. This product will be offered as a reference design.

3. 1.Key features

Here key features are divided into three categories: processing, interaction and audiovisual.

3.1.1). Processing

Dual-core 1.2 GHz ARM Processor with 1 GB of on-board memory, Android operating system (hopefully version 4.0 Ice Cream Sandwich), Embedded 3D and graphics accelerators, External SD card extension, Bluetooth and WiFi connectivity for peripherals and networks, libSensics API that provides full access to on-board capabilities.

3.1.2). Interaction

Head tracking: yaw/pitch/roll and X/Y/Z acceleration, First person hand tracking in a limitless area,120 Hz head tracking updates, 60 Hz hand tracking updates.

3. 1.3).Audiovisual

Dual SXGA (1280×1024) OLED displays, support for 720p, embedded high-performance stereo headset and embedded microphone.

3. 2. Evaluation

- The brief test was impressive - the graphics were smooth and the tracking of your head and body movements, as well as your hands in front of the camera, crisply responsive. The unit isn't as ungainly as it looks once adjusted correctly, although when jumping from rooftops during the game (which involved physically jumping) the bulk of the headset did hit home. There is clearly huge potential here though.
- Battery life - Natalia can run off rechargeable batteries or off a standard 5V power supply. Depending on the application, the batteries typically hold 1.5 to 2 hours before recharge. There are two batteries inside Natalia and they are hot-swappable, meaning that you can replace one while the other one is used to power the device.

IV. APPLICATIONS

Although the Smart Goggles clearly cater towards the needs of gamers, Sensics envisions its head gear - in this and smaller versions being used for military and professional applications[8].

4. 1. 3D Gaming Applications

When a Motorola Droid Razr was paired with the Smart Goggles, a 3D gaming application was running on the Droid, and the Smart Goggles were used both as a display mechanism – to show the 3D video – as well as an input device which captured the user's head movements and sent them to the phone. Thus it is having a great scope in the gaming field. Since they are not bulky and it is easy to make body movements. It gives you a fully immersive and enjoyable experience.

Unlike traditional goggles that, at best, provide head motion tracking and rely on external devices for user input, these goggle provide real-time, first-person tracking of the user's hands. This offers a natural way to interact with content, games, and applications. First-person hand tracking can go anywhere with the goggle, providing limitless tracking area.

4. 2.Military applications

This technology has a great potential in military field too. Various devices surrounding the goggles can be tracked by them and their applications can be run on the goggles. It makes communication faster and easier. Further more various applications can be accessed on the goggles simultaneously. Most companies working on smart glasses got started building systems for the military.

- Lumus's technology is used by pilots in the U.S. Air Force and U.S. National Guard.
- Vuzix got started working on pilot goggles for the U.S. Air Force that overlaid a preview of a weapon's blast radius onto the place being targeted, to increase awareness of potential collateral damage.

Thus in coming future we would be fulfilling most of the technological requirements of the military.

4. 3.Augmented reality applications

The software needed to offer heads-up augmented reality is far ahead of the hardware. Various augmented reality apps for smart phones can already recognize markers, text, or even landmarks in front of a device's camera and respond by overlaying text or visuals onto a view of a scene.

One example of this type of augmented reality at CES was Aurasma, a division of software company Autonomy. Aurasma's app can recognize images or landmarks and add virtual 3-D objects, for example showing dragons circling London's Big Ben to promote a Harry Potter movie. The app has been downloaded over two million times.

Aurasma can also recognize hand gestures, making virtual content interactive—a feature that would be valuable in smartgoggles. What we've got today would work just as well with goggles if they were available.

4. 4. Networking

An interactive environment in which immersive or see-through goggles include an on-board processor with 3D graphics accelerators that are as powerful as the latest tablets or cell phones. Smart Goggles can run practically any Android application, connect to the cloud, and communicate with a wide range of surrounding devices. An open operating system, Android 4.0 in the first product, that allows access to numerous applications as well as allows executing them locally – on the goggles. At the same time, maintain traditional goggle functions such as 3D viewing, head tracking and the ability to connect to external video sources.

V. CHALLENGES TO WORK ON

Despite of so many positive points, there are some limitations too which require to be be removed for better uability. We ran into some unforeseen problems, but we are working to overcome these problems and mitigate the time and money consequences of those problems.

5. 1. Battery cell performance

Batteries used by these goggles are not so durable. A battery's characteristics may vary over load cycle, over charge cycle, and over lifetime due to many factors including internal chemistry, current drain, and temperature. That batteries have a finite life is due to occurrence of the unwanted chemical or physical changes to, or the loss of, the active materials of which they are made. It depends on temperature, pressure, voltage effects and depth of discharge and charging level. The relation between the cycle life and the depth of discharge appears to be logarithmic as shown in the graph below.

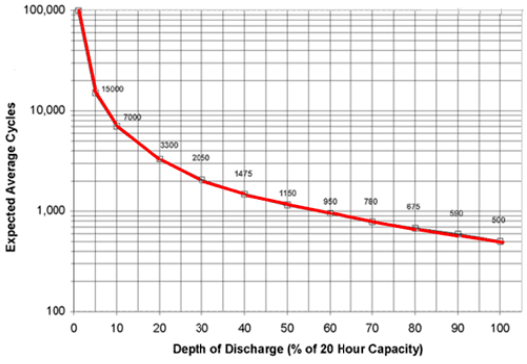

Fig. 2 : Relation between the cycle life and the depth of discharge

Thus better battery management techniques are required for their long use.

5. 2. Cost expectations

If the hype surrounding VR would not be as present, and people would be more aware (and realist) about the real promises and costs of VR, then the whole VR market would probably do much better. The problem is not so much that people see VR as something that cost little. It is more about expectations, fuelled by the hype surrounding VR that literally brainwashed decades of individuals interested by this technology. The problem we face now is to reverse that conception people have of VR, programmed deep down their brains. The hype around VR had the consequence that people started to think that the possibilities with VR are limitless. While we can pretty much say that the sky is the limit in terms of what we can currently simulate with a VR system, the problem is that it will inadvertently cost more and more as we raise the VR system's specifications to match these expectations.

5. 3. Cost with increasing resolution

A VR system requiring over 120 degrees of horizontal field of view or more will require an HMD or curved screen dome that can accommodate this. This would cost anything from USD$ 80,000 and up in 2006. To be able to track a user's body in a volume typically cost anything from a few thousands to tenths of thousands US dollars to cover only a few cubic feet of volume. The price rapidly rises to over US$ 25,000 for larger volumes. As we can see, yes, we can do such things as to display wide field of views or track large areas, but the cost for it rapidly rise as the demands do. Worse, sometimes we have to declare vanquished. Given the current information I dispose, I have yet to see an HMD that could do the 210 degrees of horizontal field of view that, we humans, can cover with both eyes. It just doesn't exist at this point. Not only that, this kind of field of view would require nothing less than 12,600 pixels horizontally to provide a 1 arc per minute visual acuity (what we consider to be a 20/20 eye sight). That is over 5 times more pixels that the maximum HDTV formats currently available. Does it means that we should just give up using an HMD? Absolutely not! We can often do pretty well without having the full human field of view covered. Said differently, there is always (or almost always) a way to find a compromise that suits their needs while being accessible on their budget.

5. 4. Eye strain

Eye-strain is typically encountered when the eye is forced to adjust rapidly to different 3D depths. This can be alleviated somewhat as content developers continue adapting to the 3D medium and learn what techniques are least troublesome to the eye.

VI. CONCLUSIONS

- Battery management systems should be employed for longer battery life so that these can be used for longer periods with ease.
- The head unit should only focus on the senses, visual, sound, vibration, kinesis, even temperature. First three senses vision, sound and touch are already controlled in todays world. But other two senses can be worked on while simultaneously improving the existing ones.
- The cameras can remain, preferably as high spec as possible and this can also augment forward vision as another application. It can have better communication antennas.
- When going to the trouble of building something so sophisticated and high tech, it will have to have a high end processor or console. As such the costs of console have naturally high limits. Therefore, it should be as a USB hid device with the customer with his own gaming rig.
- It does remain a highly evolving field and I think both of the issues on cost mentioned previously will be resolved over time and the resolutions will have a compound effect on each other.

VII. FUTURE SCOPE

- The company is also working on see-through goggles (called Marina) to complement the immersive ones. Not only would this reduce the risk of falling over the coffee table while gaming, see-through goggles would lend themselves to a variety of AR applications.
- What Sensics is working on doing is licensing and partnering Smart Goggles technology to a range of consumer electronics companies: phone, tablet, game console and PC makers who want to either build a new 3D platform or extend an existing platform to new display, natural interaction and immersion frontiers. Our hope is that these partners will collaborate with Sensics on building exciting consumer-focused products.

For example, if SONY decided to license Smart Goggles technology and make their media viewer a smart goggle - one with full head and hand tracking, wider field of view, higher resolution, untethered, and an Android processor on board. You could immerse yourself in PlayStation games, or even play them in a limitless and omni-directional tracking area. Or, you could connect to a SONY tablet or XPERIA or VITA and add intelligence, immersion and 3D to all the nice features that already exist on these devices.

- Smart Goggles represent a dramatic departure from existing goggles, which are essentially a monitor on your head. “Imagine being able to use hand movements and gestures to wield a light saber in a game, to select a movie from a media library, or to interact with augmented reality content,”. “Just like the iPhone allowed us to take our applications and media library anywhere and interact with it in a useful way, we are excited by the opportunities that the Smart Goggles offer for portable, natural, and immersive 3D interaction.”

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Implementation of DSSS Based CDMA Transmitter and Receiver Using Gold Code for FPGA

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Abstract - Direct Sequence Spread Spectrum(DS-SS) is getting great deal of prominence in wireless communication. Spread Spectrum system combined with Code Division Multiple Access (CDMA) forms a multiuser system with minimum interference.In a DS-SS system, each user is assigned a unique code sequence that allows the user to spread the information signal across the assigned frequency band. Signals from the various users are separated at the receiver by cross correlation of the received signal with each of the possible user code sequences. In this paper Direct sequence principle based CDMA transmitter and receiver is implemented in VHDL for FPGA.Transmitter module mainly consists of clock divider,data latch,Gold sequence generator and the modulo 2 adder. The receiver module consists of Mutiplier Accumulator Circuit (MAC), Gold sequence generator,comparator and a threshold block. Here, in this paper,we are using gold sequence for spreading at the transmitter and receiver.Modelsim ,Xilinx ISE-12.2 tool will be used for functional simulation and logic verification at each block level and system level. The Xilinx Synthesis Technology (XST) of Xilinx ISE tool will be used for synthesis of transmitter and receiver on FPGAs.

Keywords- *Code Division Multiple Access(CDMA),Direct Sequence Spread Spectrum(DS-SS),Multiplier Accumulator Circuit(MAC)*

I. INTRODUCTION

As the wireless personal communications field has grown over the last few years, the method of communication known as spread spectrum has gained a great deal of prominence. Spread spectrum involves spreading the desired signal over a bandwidth much larger than the minimum bandwidth necessary to send the signal. It was originally developed by the military as a method of communications that is less sensitive to intentional interference or jamming by third parties, but has become very popular in the realm of personal communications recently. Spread spectrum methods can be combined with Code Division Multiple Access (CDMA) methods to create multi-user communications systems with very good interference performance.

In this paper Direct sequence principle based CDMA transmitter and receiver will be implemented in VHDL for FPGA. In the recent years the CDMA on FPGA platform has attracted attention of academic research and industry. The Spartan TM-3E family of Field-Programmable Gate Arrays (FPGAs) is specifically broadband designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The five-member family offers densities ranging from 100,000 to 1.6 million system gates. Because of their exceptionally low cost, Spartan -3E FPGAs are ideally suited to a wide range of consumer electronics applications, including access, home networking, display/projection, and digital television equipment.

II. SPREAD-SPECTRUM TECHNIQUE

As stated before, spread spectrum systems afford protection against jamming (intentional interference) and interference from other users in the same band as well as noise by "spreading" the signal to be transmitted and performing the reverse "de-spread" operation on the received signal at the receiver. This de-spreading operation in turn spreads those signals which are not properly spread when transmitted, decreasing the effect that spurious signals will have on the desired signal.

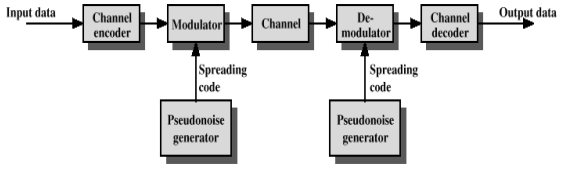

Fig. 1 Spread Spectrum System

Spread Spectrum systems can be thought of as having two general properties: first, they spread the desired signal over a bandwidth much larger than the minimum bandwidth needed to send the signal, and secondly, this spreading is carried out using a pseudorandom noise (PN) sequence. Fig. 1 shows the basic spread spectrum system.

III. DIRECT-SEQUENCE SPREAD SPECTRUM (DS-SS)

Direct Sequence Spread Spectrum (DS-SS) is the most common version of spread spectrum in use today, due to its simplicity and ease of implementation. The two major spread spectrum methods differ mainly in the way they encode the data with the PN sequence. In DSSS each user is assigned a unique code sequence (which is the PN Sequence) that allows the user to spread the information signal across the assigned frequency band.

Signals from the various users are separated at the receiver by cross correlation of the received signal with each of the possible user code sequences. Possible narrow band interference is also suppressed in this process. By designing these code sequences to have relatively small cross-correlation, the cross-talk inherent in the demodulation of the signals received from multiple transmitters is minimized.

IV. CODE DIVISION MULTIPLE ACCESS

Code Division Multiple Access (CDMA) is a spread spectrum technique that uses neither frequency channels nor time slots. With CDMA, the narrow band message (typically digitized voice data) is multiplied by a large bandwidth signal that is a pseudo random noise code (PN code). All users in a CDMA system use the same frequency band and transmit simultaneously. The transmitted signal is recovered by correlating the received signal with the PN code used by the transmitter.

CDMA technology was originally developed by the military during World War II. Researchers were spurred into looking at ways of communicating that would be secure and work in the presence of jamming. Some of the properties that have made CDMA useful are:

- Signal hiding and non-interference with existing systems.
- Anti-jam and interference rejection
- Information security
- Accurate Ranging
- Multiple User Access
- Multipath tolerance

V. DS-CDMA System

In a DS-SS system, each user is assigned a unique code sequence that allows the user to spread the information signal across the assigned frequency band. Signals from the various users are separated at the receiver by cross correlation of the received signal with each of the possible user code sequences. Possible narrow band interference is also suppressed in this process. By designing these code sequences to have relatively small cross-correlation, the cross-talk inherent in the demodulation of the signals received from multiple transmitters is minimized. This multiple access method is CDMA, which is a form of a DSSS system [4]. This modulation transforms an information bearing signal into a transmission signal with a much larger bandwidth. This transformation is achieved by encoding the information signal with a code signal that is independent of the data and has much larger spectral width than the data signal. This spreads the original signal power over a much broader bandwidth, resulting in a lower power density. The ratio of transmitted bandwidth to information bandwidth is called the processing gain *Gp* of the DS-SS system: $Gp = Bt/Bi$, where *Bt* is the transmission bandwidth and ***Bi*** is the bandwidth of the information bearing signal.

A. DS-CDMA transmitter

The basic block diagram of DS-CDMA transmitter is as shown in fig. 2 below. The binary data signal is modulated by the code signal. This code signal consists of a number of code bits called “chips” that can be either +1 or –1. The spreaded signal is modulated by a RF carrier.

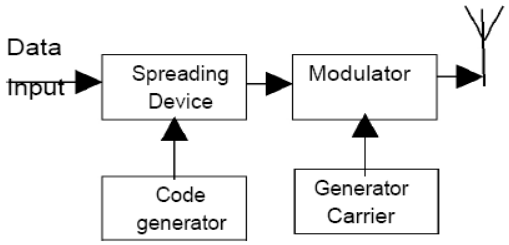

Fig. 2 Block diagram of a DS-CDMA transmitter

B. DS-CDMA receiver

After transmission of the signal, the receiver shown in Fig. 3 dispreads the SS signal using a locally generated code sequence.

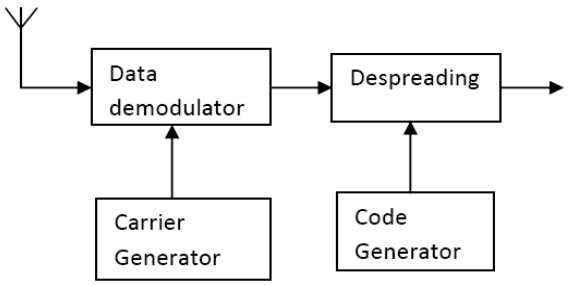

Fig. 3 Block diagram of a DS_CDMA receiver

C) **DSSS Disadvantage**

The main problem with applying Direct Sequence spreading is the so-called Near-Far effect which is illustrated in Fig. 4. This effect is present when an interfering transmitter is much closer to the receiver than the intended and B is low, the correlation between the received signal from the interfering transmitter and code A can be higher than the correlation between the received signal from the intended transmitter and code A. The result is that proper data detection is not possible.

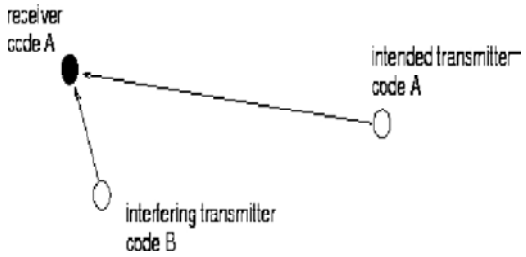

Fig. 4 Near-far effect illustrated

VI. Hardware And Software Design

A. Gold code generator

In the multi-user system, the main reason that affects the performance is the multiple access interference. Especially when the users are mobile, asynchronous and power imbalance problems emerge among the users. Because of these reasons, the selection of spreading codes to differentiate the users plays an important role in the system capacity.

For this reason, here we will use a particular class of PN sequences called as Gold sequences. They are chosen such that the cross-correlation values between the codes over a set of codes are uniform and bounded. Gold sequences have better Auto correlation over the PN sequences, thus making it more suitable for modulation and spreading of a message signal than the Pseudo Noise(PN) sequences.

Gold sequences help generate more sequences out of a pair of m-sequences giving now many more different sequences to have multiple users. Gold sequences are based on preferred pairs of m-sequences.Fig. 5 below shows the gold code generator for two polynomials: $1+x^2+x^5$ and $1+x+x^2+x^4+x^5$

m-sequences give only one sequence of length 2^5-1 . By combining two of these sequences, we can obtain up to 31 (2^5-1) plus the two m-sequences themselves, generate 33 sequences (each one length 2^5-1) that can be used to spread different input messages (different users CDMA). The m-sequence pair plus the 2^m-1 Gold sequences form the 2^m+1 available sequences to use in DSSS. The wanted property about Gold codes is that they are balanced (i.e. same number of 1 and -1s).

One of the advantages of gold code is the better Auto correlation of the Gold Codes over the PN sequences, thus Gold Code is more suitable for modulation and spreading of a message signal than the Pseudo Noise sequences.

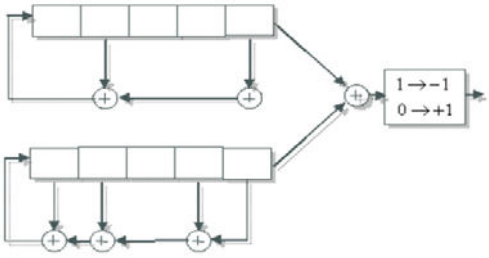

Fig. 5 Gold Sequence Generator using Preferred Pair of m-sequences : $1+x^2+x^5$ and $1+x+x^2+x^4+x^5$

B. *DS- CDMA trnsmitter*

The block diagram of CDMA transmitter which will be implemented in this project is given in the below Fig. 5. The transmitter as shown in Fig. 5 has clock divider which divides the high frequency clock for the Data latch and the Gold Code generator to work in synchronization with each other.

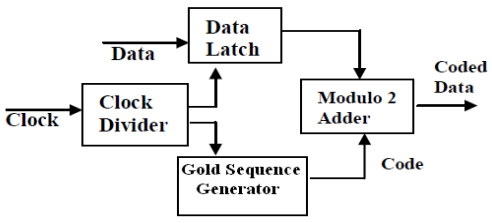

Fig. 6 CDMA Transmitter

The data latch is used to latch the input data and provide it bit by bit for modulo-2 addition to the modulo-2adder.

C. DS-CDMA receiver

Fig. 6. below shows the block diagram of CDMA receiver which will be actually implemented in this project. The receiver has Multiplier Accumulator Circuit (MAC) which performs successive addition of the input data modulo-2 added with the scrambling sequence which is used at the transmitter. The output of this MAC is given to the comparator. Gold Code Generator block is same as used in the DSSS transmitter. Threshold block is used to provide a threshold level to the incoming input bits. Setting of thresholds is done to get an exact output from an approximate output. Hence this block should be pre configured with the transmitter in order to get an approximately exact received output. The comparator compares the output of MAC with the threshold levels set at the Threshold Device.

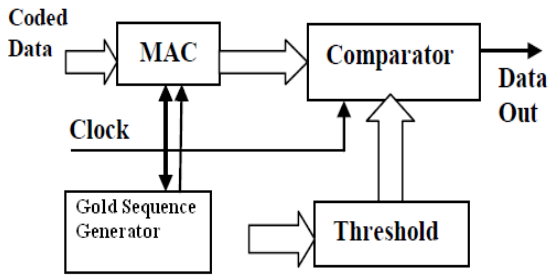

Fig. 7 CDMA Receiver

D. VHDL implementation of CDMA transmitter and receiver

A VHDL specification can be executed in order to achieve high level of confidence in its correctness before commencing design and may simulate one to two orders of magnitude faster than a gate level description. ,Xilinx ISE-12.2 tool will be used for functional simulation and logic verification at each block level and system level. The Xilinx Synthesis Technology (XST) of Xilinx ISE tool will be used for synthesis of transmitter and receiver on FPGAs.

VII. RESULT

The simulation of the entire DSSS based CDMA system will be implemented using FPGA. Till now, the results for clock divider and gold code have been obtained as shown by Fig.8 and Fig.9 below.

VIII. CONCLUSIONS

CDMA is one of the most impartant multiple access technique .In this paper the transmitter and receiver will be implemented on FPGA. This work has the following applications.

- Custom CDMA communication setup with specified PN sequence length and number of users.
- Standard CDMA systems designs such as used for mobiles and GPS.

Implementation of a CDMA communication system with

DSSS technique in VHDL has the following advantages

- The design is fully reconfigurable
- The number of bits and gold sequence can be changed very easily
- Useful for both FPGA and ASIC implementations.

Disadvantages

- Complex hardware is involved in receiver design which increases the cost of the system.

Future scope:

- The concept can be extended to design the GPS system which is CDMA system with 1023 chip length technique.

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GOLD CODE GENERATOR:

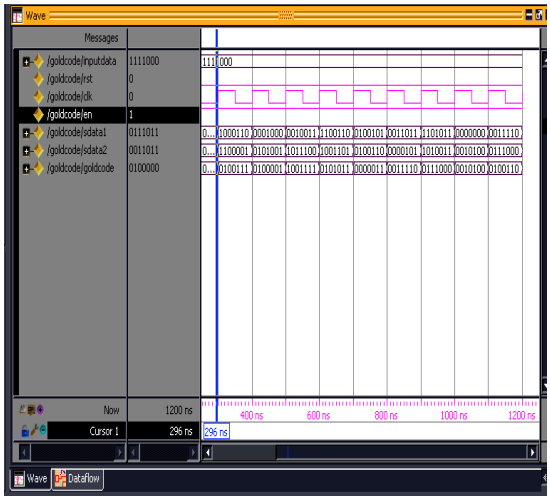

Fig. 8 Gold Code Sequence Generator output waveform
Here, Gold Sequence generated is of 7-bits

Clock Divider:

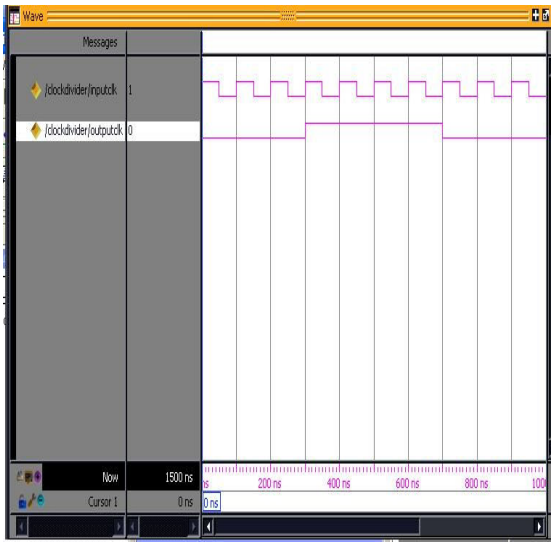

Fig.9 Clock Divider Output Waveform

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Adaptive Linear Prediction with Least Mean Square Adaptive Filter Algorithm

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Abstract - Adaptive linear Prediction is one of the most interesting applications for adaptive filters, especially for the Least Mean Square algorithm, due to its robustness and calculus simplicity. Based on the error signal, the filter's coefficients are updated and corrected, in order to adapt, so the output signal has the same values as the reference signal.. This configuration essentially performs two operations. The application enables remarkable developments and research, creating an opportunity for automation and prediction.

Keywords*:* linear prediction, adaptive Filter, Least Mean-Square (LMS) Algorithm.

I. INTRODUCTION

Filtering is the technique or practice leading to accepting selected signal from the band of spectrum of the incoming wavelengths to the system. In the process of digital signal processing, often to deal with some unforeseen signal **,** noise or time varying signals, if only by a two FIR and IIR filter of fixed coefficient cannot achieve optimal filtering. Under such circumstances, we must design adaptive filters, to track the changes of signal and noise. Digital signal processing (DSP) has been a major player in the current technical advancements such as noise filtering, system identification, and voice prediction. Standard DSP techniques, however, are not enough to solve these problems quickly and obtain acceptable results [1]. Adaptive filtering techniques must be implemented to promote accurate solutions and a timely convergence to that solution.

II. ADAPTIVE FILTER

An adaptive filter is a filter that self-adjusts its transfer function according to an optimization algorithm driven by an error signal. Because of the complexity of the optimization algorithms, most adaptive filters are digital filters [2]. Adaptive filters are required for some applications because some parameters of the desired processing operation (for instance, the locations of reflective surfaces in a reverberant space) are not known in advance. The adaptive filter uses feedback in the form of an error signal to refine its transfer function to match the changing parameters.

One of the most popular adaptive algorithms available in the literature is the stochastic gradient algorithm also called least-mean-square (LMS) [1] [2]. Its popularity comes from the fact that it is very simple to be implemented. As a consequence, the LMS algorithm is widely used in many applications. The adaptive filter uses feedback in the form of an error signal to refine its transfer function to match the changing parameters. The principle of an adaptive filter is its time varying, self-adjusting characteristics. An adaptive filter usually takes on the form of an FIR filter structure, with an adaptive algorithm that continually updates the filter coefficients, such that an error signal is minimized according to some criterion. The error signal is derived in some way from the signal flow diagram of the application, so that it is a measure of how close the filter is to the optimum. Most adaptive algorithms can be regarded as approximations to the Wiener filter, which is therefore central to the understanding of adaptive filters[3].

$$Y[n] = \sum_{k=0}^{N-1} c_k^*[n]x[n-k] \qquad (1)$$

Here, the ck[n] are time dependent filter coefficients (we use the complex conjugated coefficients ck[n] so that the derivation of the adoption algorithm is valid for complex signals, too).Adaptive filters are

designed as compare to FIR and IIR filter because in this filter coefficients are to be varied. According to taps adapt the filter by doing iterations. In this filter using a weight control mechanism or transversal filter in which weights are to be updated [4].

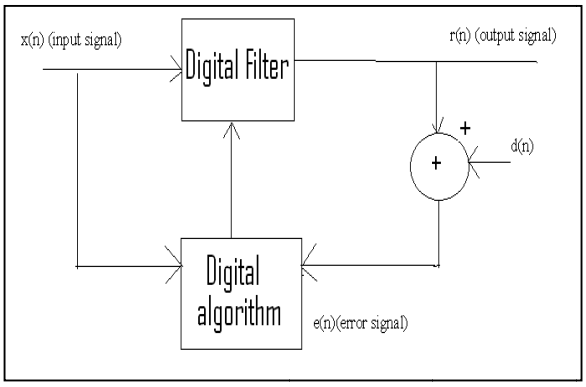

Fig1: Block diagram of adaptive filter

III. ADAPTIVE LINEAR PREDICTION CONFIGURATION

Adaptive linear prediction is one of the most interesting applications for adaptive filters. This configuration essentially performs two operations[5] [6]. The first operation, if the output is taken from the error signal e(n), is linear prediction. The adaptive filter coefficients are being trained to predict, from the statistics of the input signal x(n), what the next input signal will be. The second operation, if the output is taken from y(n), is a noise filter similar to the adaptive noise cancellation .Neither The linear prediction output nor the noise cancellation output will converge to an error of zero [7]. This is true for the linear prediction output because if the error signal did converge to zero, this would mean that the input signal x(n) is entirely deterministic, in which case we would not need to transmit any information at all. In the case of the noise filtering output, as outlined in the previous section, y(n) will converge to the noiseless version of the input signal.

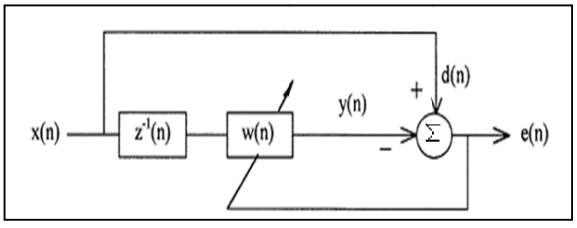

Fig-2 linear prediction configuration

IV. SIMULATION AND ANALYSIS

Fig-3 shows the input to the adaptive linear predictive coding algorithm. Fig-4 shows the output, y(t), of the adaptive LPC system representing the noise cancellation output, where it can be seen that the output is converging to a noiseless system [8] . Fig-5 shows the error signal of the LPC system.

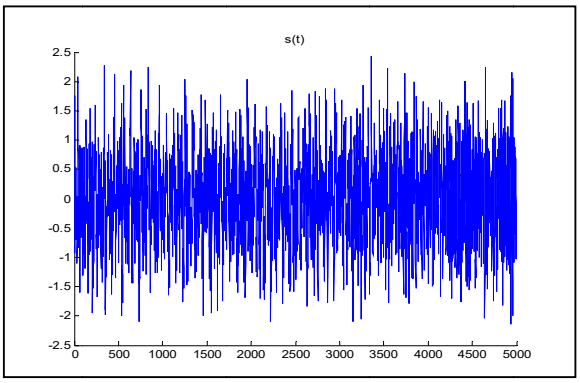

Fig- 3. Time Response of a Noisy Signal

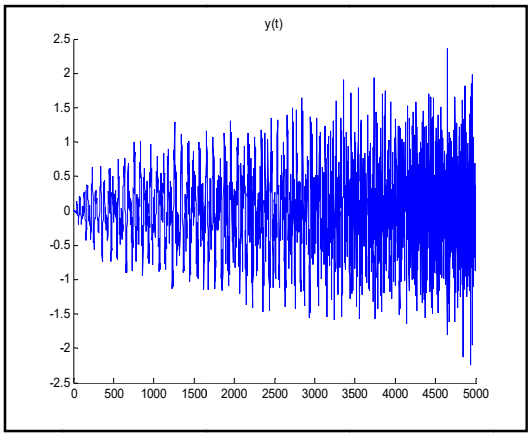

Fig-4. Time Response of the Filtered Signal.

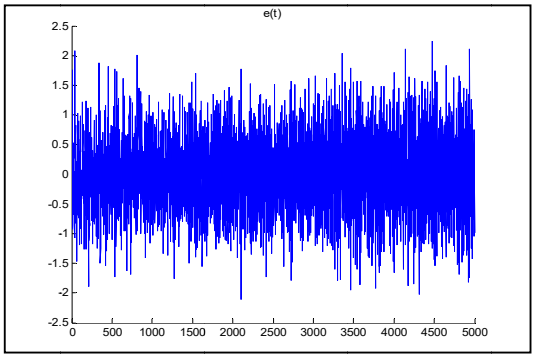

Fig- 5. Time Response of the Error Signal.

The frequency responses of each of the above inputs and outputs are given in figures 6-8. Figure 7 show that the LPC is filtering the signal. Figure 8 shows that the error signal from an LPC system has a much smaller dynamic range in the frequency domain, than does the original signal.

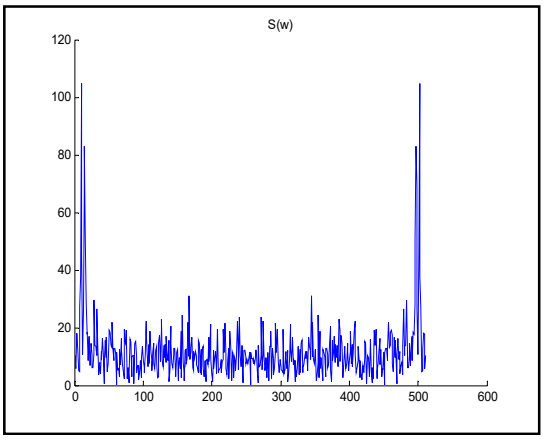

Fig- 6. Frequency Response of a Noisy Signal.

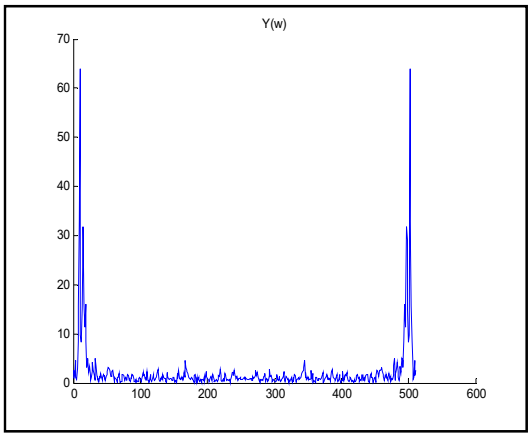

Fig- 7. Frequency Response of the Filtered Signal

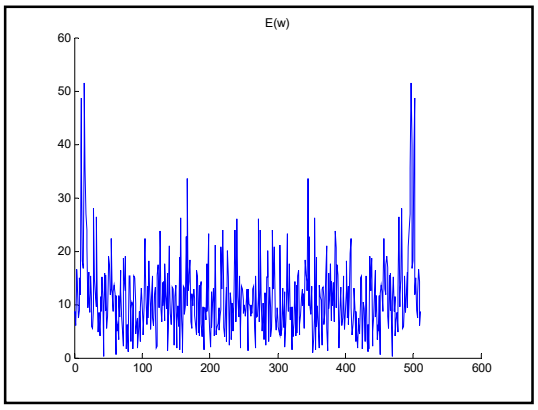

Fig- 13. Frequency Response of the Error Signal

V. CONCLUSION

Neither the linear prediction output nor the noise cancellation output will converge to an error of zero. This is true for the linear prediction output because if the error signal did converge to zero, this would mean that the input signal x(n) is entirely deterministic. Figure 8 shows that the error signal from an LPC system has a much smaller dynamic range in the frequency domain, than does the original signal.

ACKNOWLEDGMENT

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Security Issue in Progressive Transmission of Medical Images by Reducing Bandwidth in Teleradiology applications

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Abstract - Progressive transmission of medical images through Internet has emerged as a promising protocol for teleradiology applications. The major issue that arises in teleradiology is the difficulty of transmitting large volume of medical data with relatively low bandwidth. Recent image compression techniques have increased the viability by reducing the bandwidth requirement and allowing cost-effective delivery of medical images for primary diagnosis.
The increasing adoption of information systems in healthcare has led to a scenario where patient information security is more and more being regarded as a critical issue. Allowing patient information to be in jeopardy may lead to irreparable damage, physically, morally, and socially to the patient, potentially shaking the credibility of the healthcare institution. This demands adoption of security mechanisms to assure information integrity and authenticity. Structured descriptions attached to medical image series conforming to the DICOM standard make possible to fit the collections of existing digitized images into an educational and research framework.

General Terms: Transmission of Medical Images, Security Issue in Transmission, Measuring Lossless compression effectiveness ,Compression Algorithm.

Keywords *:* DICOM (Digital Imaging and Communications in Medicine) Image Compression, Lossless Compression, FWT with Daubechie's Wavelet

I. INTRODUCTION

One of the main challenges of the current medical imaging systems is dealing with large amounts of data acquired by the modern modalities. Indeed, new modalities can generate large amounts of high-quality images in a short time. In fact, one of the most important demands toward dealing with large amount of data is to provide a way for fast data transmission between medical imaging applications. The most common approach toward enhancing the speed of data transmission is using compression techniques. This approach is only effective when the speed of the connecting media is not much compared to the compression/decompression computing time, so adding the overhead of compression/ decompression times is worth. Hence, as a matter of fact, compression techniques are ineffectual in high-speed networks.

II. BACKGROUND

With the DICOM standard, it is easy to eliminate textual information such as patient name and ID.However for digitized films or previous history images, a computerized detection and elimination algorithm is needed. The problem of text identification arises in many applications other than medical security. However, the algorithms used in such systems are not designed to handle superimposed text because it is difficult to differentiate the edges of text from the edges of the medical objects in the image.The security filtering process in our system consists of an efficient and accurate algorithm to distinguish areas with and without textual information in digital or digitized medical images. Areas with text can then be blurred or striped. Because variations in the diagonal directions can be found in almost all Roman characters or Arabic numbers, we use Daubechies' wavelets and analysis techniques to detect the high frequency variation in the diagonal direction that is indicative of text. A mask is used to preserve the losslessness of non-textual areas. With some basic knowledge of the machine used to create the image, we are able to eliminate only sensitive patient identification information while retaining the medical information in the image.Excellent results have been obtained in experiments using a large set of realworld medical images many with superimposed text.

III. TRANSMISSION OF MEDICAL IMAGES

Parallel transmission between two medical imaging systems is proposed and assessed. The proposed approach is based on Digital Imaging and Communications in Medicine (DICOM) protocol. DICOM is the standard storage format as well as the transmission protocol, for medical images. It has several advantages such as interoperability, integrity and consistency, which have made it the world wide practical standard for interconnecting medical imaging systems.

The proposed method uses parallel connections to carry out the image transformation between two DICOM application entities. These parallel connections are used in the Storage Services in the DICOM protocol. In fact, the method is a way to improve the speed of data transmission in high-speed networks where data compression techniques are not effective.

IV. SECURITY ISSUE IN TRANSMISSION

Before digital medical images in computer-based patient record systems can be distributed online, it is necessary for confidentiality reasons to eliminate patient identification information that appears in the images. This requires an automatic security filtering algorithm for on-line medical image distribution using Daubechies' wavelets. With the advancements of the World-Wide Web, the Internet and medical imaging technology, it is becoming increasingly difficult to maintain and retrieve digital health care information. Besides the traditional textual data such as patient reports, health care records are being filled with X-ray images, MRI scans, CT scans, 3-D volume reconstructions and video streams.

Figure 1-Text and Non-Text areas in Medical Images

Efficient security filtering for digital medical images is desirable before medical images (Figure 1) can be transmitted to researchers and external users.

V. COMPRESSION TECHNIQUES

5.1 Lossy vs. Lossless compression

Despite advances in lossy compression, lossless compression remains useful for many medical imaging applications.It is still unclear in what situations lossy compression is appropriate for short or long term archival or for transmission for diagnostic interpretation.

Lossy Compression

Lossy compression reduces a file by permanently eliminating certain information, especially redundant information. When the file is uncompressed, only a part of the original information is still there but the user may not notice it . Lossy compression is generally used for video and sound, where a certain amount of information loss will not be detected by most users. The Joint Photographic Experts Group (JPEG) image file, commonly used for photographs and other complex still images on the Web is an image that has lossy compression. Using JPEG compression, the creator can decide how much loss to introduce and make a trade-off between file size and image quality.

Of course, with lossy compression, we can't get the original file back after it has been compressed. One get stuck with the compression program's reinterpretation of the original. For this reason, we can't use this sort of compression for anything that needs to be reproduced exactly.

Lossless Compression

With lossless compression, every single bit of data that was originally in the file remains after the file is uncompressed. All of the information is completely restored. This is generally the technique of choice for text or spreadsheet files, where losing words or financial data could pose a problem. The Graphics Interchange File (GIF) is an image format used on the Web that provides lossless compression. This is used in software applications, databases and presidential inauguration speeches,Diagonistic problems.

VI. MEASURING LOSSLESS COMPRESSION EFFECTIVENESS

The effectiveness of lossless compression schemes can be described using a relative measure, "Compression Ratio" or by describing an absolute measure the "Bit Rate" of an image. The Bit Rate is the average number of bits (fractional) required to encoded a pixel and is computed from the total number of bits encoded divided by the number of pixels. Such a value

is useful when comparing different schemes applied to one image or multiple images with the same bit depth which in the case of this study they do not. Accordingly, a relative measure, the compression ratio is used here. Compression Ratios are computed from different metrics of size.One approach common in the literature is to compare the ratio of the number of bits in the uncompressed image to the number of bits in the encoded image. In the case of eight bit images common in non-medical applications this is straightforward and provides a meaningful comparison. Unfortunately, the number of bits in an uncompressed medical image may be hard to determine. Most DICOM images contain a description of bit depth that may be considered as the "nominal" bit depth, but this may be artificially large for computing compression ratios. For example, most MR images have a nominal bit depth of 16, though the actual pixel values may be encoded in fewer bits.

VII. THE SYSTEM

The architecture of the system is shown in Figure 2

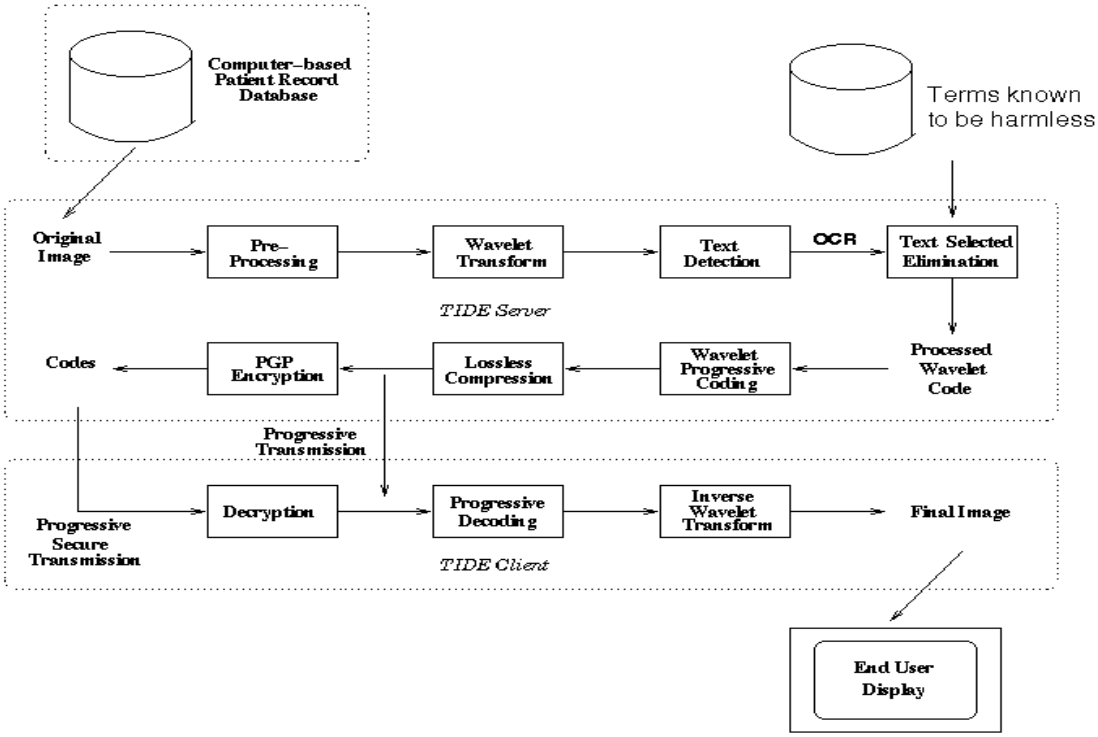

FIGURE 2-Architecture of the System

We apply an N-level fast wavelet transform (FWT) with Daubechies wavelet to each medical image where N is determined adaptively by the image size as depicted in Figure-3. If the image is of DICOM standard, we may eliminate the patient identification information without processing the image content.

For non-DICOM images, we extract and analyze the lower right-hand corners of each level of the transform matrix, where the diagonal directional high frequency information is located, to obtain a mask containing only the areas with textual information.

FIGURE 3-Text pixels extracted after processing the wavelet transform

Once such a mask is computed, we apply it to all the high-frequency bands to eliminate the text within areas with textual data. Or, we may apply the mask selectively to all the frequency bands to block the areas with text. Knowledge of the rough location (e.g.,which one of four corners) of the critical patient identification information of certain type of medical images is used to eliminate only information needed to be deleted while preserving the rest.When we do not have knowledge of the rough location of patient identification information, we may apply the mask to eliminate all textual information within the medical image as shown in Figure 4.

FIGURE 4-Patient identification information is eliminated

To achieve secure transmission, we may also apply a Pretty Good Privacy (PGP) encryption to the code segments before sending the data to the client via public network.

VIII. COMPRESSION ALGORITHM

In this paper we apply N-level Fast Wavelet Transform (FWT) with Daubechie's Wavelet to each medical image where N is determined adaptively by the image size.

Our text detection algorithm has several immediate advantages-

1. Unlike traditional approaches, such as the neural network, algorithm does not depend on the actual font size, font type and style of the text in the medical image.
2. It is proposed to use Daubechie's Wavelets rather than a traditional edge detector to capture the high frequency information in the images. This reduced the dependence of the results on the quality or the sharpness of the images.
3. The algorithm does not rely on the color of the image or the text. It also has minimum dependence on the contrast between text and background objects.
4. It is faster than other algorithms due to our adaptive multiresolution approach.
5. Wavelet-based algorithm using Daubechie's Wavelets can be easily integrated with cutting-edge image compression, compressed-domain indexing and processing algorithms.
6. Experiments indicate that the algorithm is capable of handling images with superimposed hand-written text and even foreign languages.

IX. RESULTS

In this paper, we have demonstrated an efficient wavelet-based security filtering algorithm for on-line medical image distribution. This algorithm has been implemented by testing about 75 medical images of different modalities,collected from different sources. Some of them are downloaded from the world-wide web and medical imaging newsgroups. The textual information detection and elimination module takes about 1 second of CPU time to process a 12-bit medical image of size 512 x 512. The algorithm is a linear algorithm with respect to the size of the image. Besides the fast speed, the algorithm has achieved remarkable accuracy. It successfully detected and eliminated all of the critical textual information within the corners of the medical images.

X. ACKNOWLEDGEMENTS

I would like to thank Mrs.Mukta Bhatele,Professor,Computer Science,Gyan Ganga College of Technology,Jabalpur for valuable help and discussions.I sincerely express indebtedness to esteemed and revered guide Prof.Mukta Bhatele for their invaluable guidance, supervision and encouragement throughout the work. Without her kind patronage and guidance the project would not have taken shape.I would like to express our sincere regards to her for advice and counseling from time to time. I also thanks APEX Hospital and Research Center, Jabalpur for its contribution to the collection of images used.This study would not have been possible if compression researchers did not routinely place their code and papers on the Internet for public access.

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A Novel Still Image Mosaic Algorithm Construction Using Feature Based Method

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Abstract - An image mosaic is a method of assembling multiple overlapping images of same scene into a larger one. The output of image mosaic will be the union of two input images. In this paper we have to use three step automatic image mosaic method. The first step is taking two input images and finding out the corners in both the images, second step is finding its matched corner and third step is its blending and we get final output mosaic. The experimental results show the proposed algorithm produces an improvement in mosaic accuracy, efficiency and robustness.

Keywords - *Mosaicing, Registration, Stitching, Warping, Blending.*

I. INTRODUCTION

Image mosaicing is a process of assembling images of same scene into a large image. The output of image mosaicing operation will be the union of two input images. An Image mosaic is a synthetic composition generated from a sequence of images and it can be obtained by understanding geometric relationships between images. The geometric relations are the coordinate system that relate the different image coordinate systems. By applying the appropriate transformations via a warping operation and merging the overlapping regions of warped images, it is possible to construct a single image indistinguishable from a single large image of the same object, covering the entire visible area of the scene. This merged single image is the motivation for the term *mosaic*.

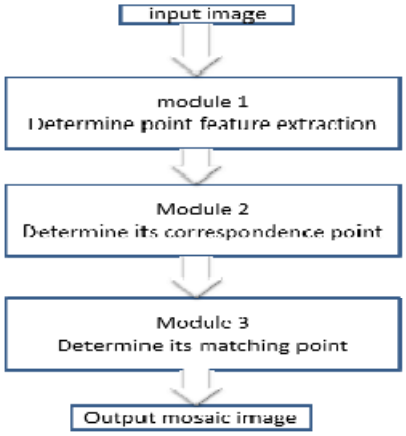
Various steps in mosaicing are feature extraction and registration, stitching and blending. Image registration refers to the geometric alignment of a set of images. The set may consist of two or more digital images taken of a single scene at different times, from different sensors, or from different viewpoints. The goal of registration is to establish geometric correspondence between the images so that they may be transformed, compared, and analyzed in a common reference frame. This is of practical importance in many fields, including sensing, medical imaging, and computer vision.

Registration methods can be loosely divided into the following classes: algorithms that use image pixel values directly, e.g.,correlation methods [2]; algorithms that use the frequency domain, e.g., Fast Fourier transform based (FFT-based) methods [3]; algorithms that use low level features such as edges and corners, e.g., Feature based methods [1]; and algorithms that use high-level features such as identified (parts of) objects, or relations between features, e.g., Graph-theoretic methods[1].

The next step, following registration, is image stitching. Image integration or image stitching is a process of overlaying images together on a bigger canvas. The images are placed appropriately on the bigger canvas using registration transformations to get the final mosaic. At this stage, the main concerns are in respect of the quality of the mosaic and the time efficiency of the algorithm used.

Image Blending is the technique, which modifies the image gray levels in the vicinity of a boundary to obtain a smooth transition between images by removing these seams and creating a blended image by determining how pixels in an overlapping area should be presented. The term *image spline* refers to digital techniques for making these adjustments. A good image spline makes the seam perfectly smoth, yet preserves as much as the original information as possible.

II. DESIGN METHODOLOGY



III. FEATURE POINT EXTRACTION

A) The Idea of Harris Corner

The first step in the image mosaic process is feature detection. Therefore we introduce Harris detector in our mosaic framework. Harris Corner detecting was a point feature extracting algo based on Moravec algorithm by C.Harris and M.J Stepens in 1988. Its main idea is to design a local detecting window in image. when the window moves in each direction the average grey variation of the window is more than threshold, then the center point of the window is extracted as corner point. When we just shift one pixel in an image that can create a significant change in the corner.

Let the grey of pixel (u,v) be I(x,y) then the grey variation of pixel (x,y) with a shift (u,v) can be denoted as :

$$E(u,v)=\sum_{x,y} w(x,y)\left[I(x+u,y+v)-I(x,y)\right]^2$$

Applying Taylor series expansion we get,

$$E(u,v)=\sum_{x,y} w(x,y)[I(x+u,y+v)-I(x,y)]^2$$

$$=\sum_{x,y} w(x,y)[I_u u+I_v v+O(u^2,v^2)]^2$$

For small shifts [*u, v*] we have the following approximation,

$$E(u,v)\cong \begin{bmatrix} u & v \end{bmatrix} M \begin{bmatrix} u \\ v \end{bmatrix}$$

Where *M* is a 2×2 matrix computed from image derivatives:

Measure of corner response:

$$M=\sum_{x,y} w(x,y)\begin{bmatrix} I_x^2 & I_xI_y \\ I_xI_y & I_y^2 \end{bmatrix}$$

Let λ_1, λ_2 be the eigen values of M, then the flat area, corner and edge of the image can be detect by the eigen values as followed.

- Flat area: both λ_1, λ_2 are tiny.
- Edge: one of λ_1, λ_2 is smaller and the other is bigger.
- Corner: both λ_1, λ_2 are bigger and are nearly the equal.

To extract the corner, Harris constructed the formula as:

$$R=\det M-k\left(\operatorname{trace} M\right)^2$$

$$\det M = \lambda_1\lambda_2$$

$$\operatorname{trace} M = \lambda_1+\lambda_2$$

IV. COMPUTING HOMOGRAPHIES

A) RANSAC algorithm:

First of all we need to know what RANSAC (Random Sample Consensus) actually mean before going into the details of homography. Generally we use RANSAC algorithm for fitting of models in presence of many available data outliners in a robust manner. Given a fitting problem with parameters $\vec{x}$, it estimates the parameters considering the following assumptions.

1. Parameters can be estimated from N data items.
2. Available data items are totally M.
3. The probability of a randomly selected data item being part of a good model is P_g.
4. The probability that the algorithm will exit without finding a good fit if one exists is P_{fail}.

Then, the algorithm:

1. Selects N data items at random
2. Estimates parameter $\vec{x}$
3. Finds how many data items (of *M*) fit the model with parameter vector $\vec{x}$ within a user given tolerance. Call this *K*.
4. If *K* is big enough, accept fit and exit with success.
5. Repeat 1..4 *L* times
6. Fail if you get here

How big *K* has to be depends on what percentage of the data you think belongs to the structure being fit and how many structures you have in the image. If there are multiple structures then, after a successful fit, remove the fit data and redo RANSAC.

We can find *L* by the following formulae:

P_{fail} = Probability of L consecutive failures

P_{fail} = (Probability that a given trial is a failure)L

P_{fail} = (1 - Probability that a given trial is a success)L

P_{fail} = (1 - (Probability that a random data item fits the model)N)L

$$P_{fail} = (1 - (P_g)^N)^L$$

$$L = \frac{\log(P_{fail})}{\log(1-(P_g)^N)}$$

B) Homography:

It's nothing but a mapping between two spaces which often used to represent the correspondence between two images of the same scene. It's widely useful for this project where multiple images are taken from a rotating camera having a fixed camera center ultimately warped together to produce a panoramic view.

Let's take a situation of projection transformation of planes in images. We have two cameras *C*1 and *C*2 looking at a plane π in the world. Consider a point *P* on the plane π and its projections.

$p = (u1, v1, 1)^T$ in *image*1 and $q = (u2, v2, 1)^T$ in *image*2.

There exists a unique (up to scale) 3 × 3 matrix *H* such that, for any point *P*:

$$q \equiv Hp \qquad (1)$$

(Here ≡ implies the left and right hand sides are proportional and those homogeneous coordinates are trivially equal)

As mentioned earlier H only depends on the plane and the projection matrices of the two cameras and being a projective transformation matrix can be only defined up to a scale.

Lastly to say, as *q* and *Hp* are only *proportional* to each other so equivalently we have

$$q \times Hp = 0 \qquad (2)$$

This H is a *projective* transformation of the plane, also referred to as a *homography*.

Since the matrix H has 8 DOF, 4 point correspondences determine H.

Thus, H is estimated with a minimization scheme using:

h = (h11; h12; h13; h21; h22; h23; h31; h32; h33)T (3)

N point correspondences give 2N linear constraints, using (2). This results in a system of the form Bh = 0.

The following problem must then be solved:

$$\min_h ||Bh|^2 \text{ subject to} ||h|| = 1 \qquad (4)$$

The Homography Detection Algorithm using RANSAC scheme

1. First corners are detected in both images.
2. Variance normalized correlation is applied between corners, and pairs with a sufficiently high correlation score are collected to form a set of candidate matches.
3. Four points are selected from the set of candidate matches, and a homography is computed using (2).
4. Pairs agreeing with the homography are selected. A pair (p, q), is considered to agree with a homography H, if for some threshold [2]:

   dist (Hp, q) < $\in$
5. Steps 3 and 4 are repeated until a sufficient number of pairs are consistent with the computed homography.
6. Using all consistent correspondences, the homography is recomputed by solving (4).

V. IMAGE WARPING AND BLENDING

A) Image warping

The last step is to warp and blend all the input images to an output composite mosaic. Basically we can simply warp all the input images to a plane defined by one of them known as reference image. The output in this case is known as composite panorama.

1. First we need to make out the output mosaic size by computing the range of warped image coordinates for each input image, as described earlier we can easily do this by mapping four corners of each source image forward and computing the minimum *x*, minimum *y*, maximum *x*, and maximum *y* coordinates to determine the size of the output image. Finally x-offset and y-offset values specifying the offset of the reference image origin relative to the output panorama needs to be calculated.

2. The next step is to use the inverse warping as described above for mapping the pixels from each input image to the plane defined by the reference image, is there to perform the forward and inverse warping of points, respectively.

B) Image blending:

The final step is to blend the pixel colors in the overlapped region to avoid the seams. Simplest available form is to use feathering, which uses weighted averaging color values to blend the overlapping pixels. We generally use alpha factor often called alpha channel having the value 1 at the center pixel and becomes 0 after decreasing linearly to the border pixels. Where at least two image overlap occurs in an output mosaic we will use the alpha values as follows to compute the color at a pixel in there, suppose there are 2 images, $I1$, $I2$, overlapping in the output image; each pixel (x, y) in image I_i is represented as $I_i(x, y) = (\alpha iR, \alpha iG, \alpha iB, \alpha j)$ where (R, G, B) are the color values at the pixel. We will compute the pixel value of (x, y) in the stitched output image as $[(\alpha 1R, \alpha 1G, \alpha 1B, \alpha 1) + (\alpha 2R, \alpha 2G, \alpha 2B, \alpha 2)] / (\alpha 1+\alpha 2)$.

VI. EXPERIMENT

The algorithm proposed in the paper has been implemented in Matlab 7.1 fig 2 shows the result of image mosaic of the experiment. Fig (a) and Fig (b) is an input image. Fig 2(a) and 2(b) is the corner detecting result of image (a) and image (b) by using Harris corner detecting algorithm. In the experiment the sum of matched corner pair is 220 and the correct matched pair is 190 .The efficient matched ratio is about 95% . As shown in fig the result of image mosaicing and image fusion is effective.

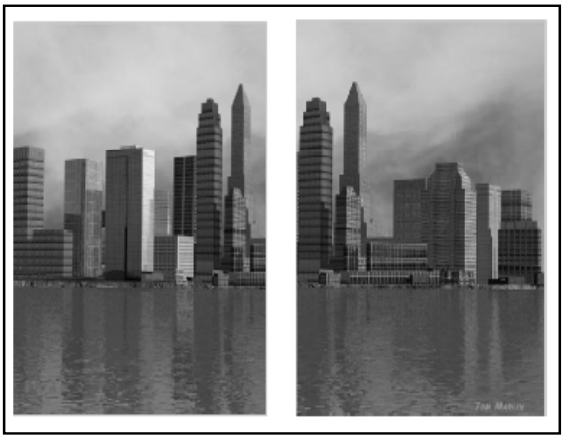


Image (a) Image (b)

Corner in : Image(a) Image (b)

Final output Mosaic Image

VII.CONCLUSION

An Harris corner detecting method is proposed to extract the corner which need not set the threshold by manual and is in sensitive to isolated point, noise and edge. So it can avoid corner redundant or lost brought by uncertain threshold selection and improve the precision of corner detecting more ever by using the advantage of RANSAC in parameter estimation, which can remove the false matched corner pair effectively and improve the corner matched ratio. Experiment shows the proposed algorithms has achieved well result.

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Data Aggregation in Wireless Sensor Network : A Survey

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Abstract - the fast advancement of hardware technology has enabled the development of tiny and powerful sensor nodes, which are capable of sensing, computation and wireless communication. This revolutionizes the deployment of wireless sensor network for monitoring some area and collecting regarding information. However, limited energy constraint presents a major challenge such vision to become reality. Data communication between nodes consumes a large portion of the total energy consumption of the WSNs. Consequently, Data Aggregation techniques can greatly help to reduce the energy consumption by eliminating redundant data traveling back to the base station (sink).This paper signifies the various data aggregation techniques in wireless sensor network and survey of data aggregation techniques in wireless sensor networks. The main goal of data aggregation is to gather and aggregate data in an energy efficient manner so that network lifetime is enhanced.

Keywords- *Wireless Sensor Network, Sensor Node, Data Aggregation, Sink, Survey.*

I. INTRODUCTION

WSNs Networked devices that are capable of sensing, computing & communicating. WSNs consist of many sensor nodes and one or more base station (BS) or sink. . Wireless sensor nodes are very small in size and have limited processing capability with very low battery power this restriction of low battery power makes the sensor network prone to failure. It has also a sensing element and a transceiver. Sensor nodes sense the physical environment periodically, process it and send the data in the form of signals to the base station. WSN is a fast growing technology. These networks have huge application. Monitoring, disaster management, security and military etc. The frequency of data reporting and the number of sensors which report data usually depends on the specific application. Wireless sensor networks are new class of distributed systems that are an integral part of the physical space they inhabit [1]. WSN technology has the capability of quick capturing, processing, and transmission of critical data in real-time with high resolution. WSN is an emerging field with many applications in almost all walks of life. As soon as people understand the capabilities of a wireless sensor network, hundreds of applications spring to mind.

Basic features of sensor networks are self-organizing capabilities, dynamic network topology, limited power, node failures & mobility of nodes, short-range broadcast communication and multi-hop routing, and large scale of deployment. The strength of wireless sensor network lies in their flexibility and scalability. The capability of self-organize and wireless communication made them to be deployed in an ad-hoc fashion in remote or hazardous location without the need of any existing infrastructure. Through multi-hop communication a sensor node can communicate a far away node in the network. This allows the addition of sensor nodes in the network to expand the monitored area and hence proves its scalability & flexibility property.

The basic goals of a WSN are to [2]:

- Determine the value of physical variables at a given location.
- Detect the occurrence of events of interest, and estimate parameters of the detected event or events
- classify a detected object
- Track an object.

Figure 1 shows a typical sensor network deployment. Each of these sensor nodes has the capabilities to collect data and route data back to the sink. The sensors coordinate among themselves to form a communication network such as a single multi-hop network or a hierarchical organization with several clusters and cluster heads. While sending the data by its transceiver some amount of energy is consumed. Sensor nodes have less amount of energy so energy conservation is the important factor in sensor network.

However, because sensors have severe resource constraints in terms of power, processing capability, memory and storage. it is challenging to provide

efficient solutions to the data-gathering problem. Energy limitations have been an especially pressing issue that affects the design of WSNs at all layers of the protocol stack. There are various mechanisms such as shutting down the radio, eliminating control packets, and using topology-management algorithms to reduce energy consumption in WSNs. Data aggregation is also among those mechanisms utilized to save energy and achieve energy efficiency.

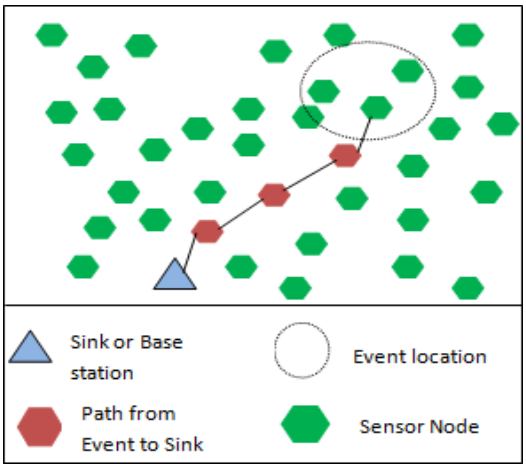

Figure1 A typical sensor network deployment

II. DATA AGGREGATION :AN OVER VIEW

Data Aggregation Technique explores how the data is to be routed in the network as well as the processing method that are applied on the packets received by a Node. Data Gathering or Data Aggregation is the process of systematically sensed data from the multiple sensor nodes to base station.

For instance, WSNs may have a lot of redundant data because multiple sensors can sense similar information when they are close to each other. Therefore, there is no need to send the same information to the BS more than once when a summary of the readings from those sensors can be sent. Thus, data aggregation will decrease the number of transmissions in the network, eventually reducing the bandwidth usage and eliminating unnecessary energy consumption in both transmissions and receptions. Data Aggregation may help reduce the number of transmissions and hence energy consumption. It may adversely affect other performance metrics such as delay, accuracy, and security [3]. If we aggregate the data before reaching the base station we can potentially decrease the number of packets in the network so we will have to send less number of packets to base station and that can save the energy of sensor nodes. These types of data aggregation are called In-Network data aggregation where packets are combined before reaching the base station. Data Aggregation in WSNs is done by the intermediate nodes en route to the BS incrementally; it is usually referred as in-network Data Aggregation [3]. Figure 2. (a) Shows no Data Aggregation model and six transmissions (b) with Data Aggregation model with four transmissions.

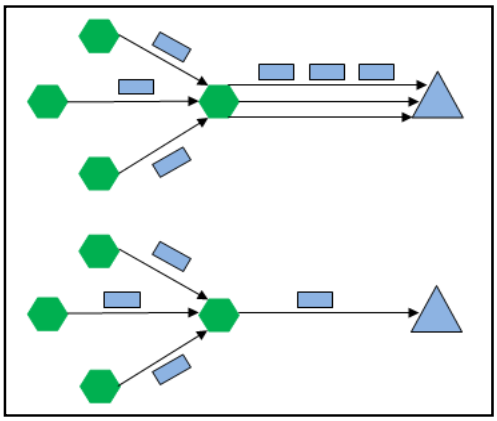

Figure 2 (a) No Data Aggregation model and six transmissions (b) With Data Aggregation model with four transmissions [3]

They have a great impact on the energy consumption of nodes and thus on Network efficiency by reducing number of transmission or length of packet. Elena Fosolo *et al.* in [4] defines the in-network aggregation process as follows: "In-network aggregation is the global process of gathering and routing information through a multi-hop network, processing data at intermediate nodes with the objective of reducing resource consumption (in particular energy), thereby increasing network lifetime." Figure 2 shows how data aggregation provides energy efficiency. Figure 3 shows effect of data aggregation.

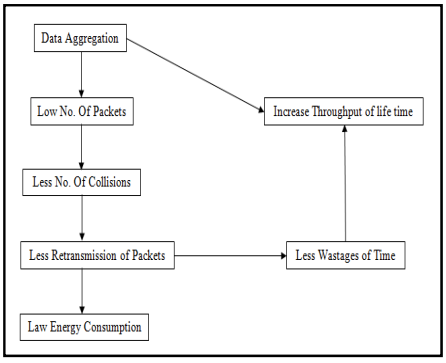

Figure 3 Effect of Data Aggregation

III. TECHNIQUES OF DATA AGGREGATION IN WSN

The Techniques of Data Aggregation are divided into two parts: structure based and structure free. Structure based data aggregation can be further divided into four parts flat network based, cluster based, tree based and grid based. Figure 4 shows classification of Data Aggregation techniques.

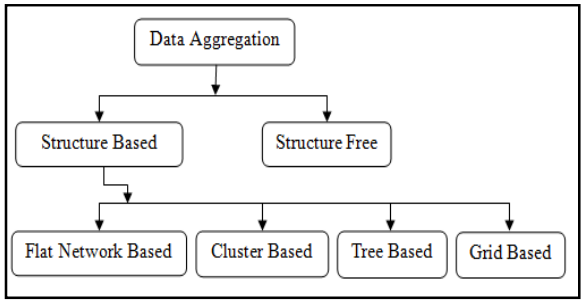

Figure 4 Classification of Data Aggregation Techniques [5]

A. Strucure Based

a) Data Aggregation in Flat Network Based

In this type of network each sensor node have the same function and capable of performing with almost the same battery power. In such networks, data aggregation is achieved by data centric routing where the sink or base station usually transmits a query message to the sensors, for example, via flooding and sensors which have data matching the query send response messages back to the sink.

b) Data Aggregation in Hierarchical Network

A flat network can result in excessive communication and computation burdens at the sink node, resulting in a faster depletion of its battery power [6]. The death of the sink node breaks down the functionality of the network. Hence, in view of scalability and energy efficiency, several hierarchical data-aggregation approaches have been proposed. Hierarchical data aggregation [6] involves data fusion at special nodes, which reduces the number of messages transmitted to the sink. This improves the energy efficiency of the network. Cluster, tree and grid networks come under hierarchical topology, which we discuss in the following section.

c) Data Aggregation in Cluster Based

The process of grouping the sensor nodes in large-scale sensor network is known as clustering. The way to combine and compress the data belonging to a single cluster is known as data aggregation in cluster based environment. Such a large size and energy restricted sensor networks, it is inefficient for sensors to transmit the data directly to the base station. In such scenarios, the network is divided into several clusters, where each cluster is managed by cluster head (CH). The sensor nodes can transmit data to a cluster head which aggregates data from all the sensors in its cluster and transmits to the base station. This results in energy savings for the energy restricted sensor nodes. Figure 5 shows a cluster based sensor network. The cluster heads can communicate with the sink directly via long range transmissions or multi hoping through other cluster heads.

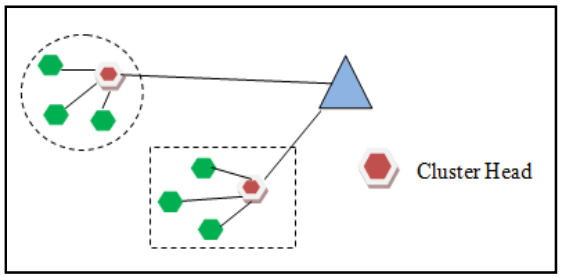

Figure 5 Cluster based sensor network

d) *Chain-Based Data Aggregation*

In cluster-based approach, sensor nodes send data to the cluster head where data aggregation process is performed. However, if the cluster head is far away from the sensor nodes, so the energy consume in communication. Further improvements in energy efficiency can be obtained if sensors transmit only to close neighbors. The idea behind chain-based data aggregation is that each sensor transmits only to its closest neighbor. The nodes can form a chain by employing a greedy algorithm or the sink can determine the chain in a centralized manner. Greedy chain formation assumes that all nodes have global knowledge of the network. The farthest node from the sink initiates chain formation and, at each step, the closest neighbor of a node is selected as its successor in the chain. In each data-gathering round, a node receives data from one of its neighbors, fuses the data with its own, and transmits the fused data to its other neighbor along the chain. Eventually, the leader node which is similar to cluster head transmits the aggregated data to the sink. Figure 6 shows the chain-based data-aggregation procedure. Nodes take turns in transmitting to the sink. The greedy chain formation approach used in may result in some nodes having relatively distant neighbors along the chain.

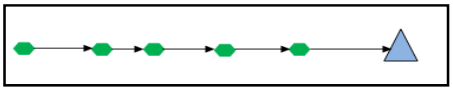

Figure.6 Chain based data aggregation

e) Tree-Based Data Aggregation

In a tree-based network, sensor nodes are formed into a tree where data aggregation is carry out at intermediate nodes along the tree and a compact representation of the data is transmitted to the sink node consider as a root node and source consider as a leaves node as shown in the Figure 7. Information flowing of data start from leaves node up to root. Tree-based data aggregation is suitable for applications which involve in-network data aggregation. An example application is radiation level monitoring in a nuclear plant where the maximum value provides the most useful information for the safety of the plant. One of the main aspects of tree-based networks is the construction of an energy efficient data aggregation tree. Various tree data aggregation algorithms have been proposed in the literature.

An energy-aware spanning tree algorithm, E-Span [7]. Marc Lee et al. proposed an energy-aware spanning tree algorithm for data aggregation, referred as E-Span. E-Span is a distributed protocol in which source node that has highest residual energy is chosen as root. Other source nodes choose their parent based on residual energy and distance to the root. The protocol uses configuration message to exchange information of node i.e., residual energy and distance to the root. Each node performs single-hop broadcast operation to send packets. Single-hop broadcast refers to the operation of sending a packet to all single-hop neighbors.

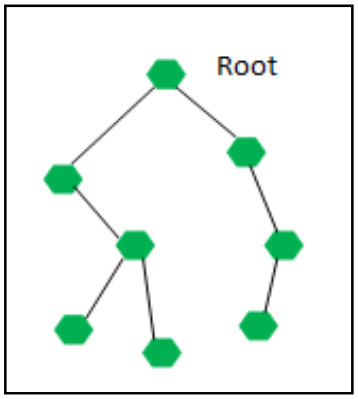

Figure.7 tree based Data Aggregation

f) Grid-Based Data Aggregation.

In grid-based data aggregation, a set of sensor nodes are assigned as data aggregators in fixed regions of the sensor network. The sensors in a particular grid transmit the data directly to the data aggregator of that grid. Hence, the sensors within a grid do not communicate with each other. In-network aggregation is similar to grid-based data aggregation with two major differences, namely, each sensor within a grid communicates with its neighboring sensors. Any sensor node within a grid can assume the role of a data aggregator in terms of rounds until the last node dies. [8].

B. Structure Free Based

In structure free data aggregation we do not maintain any structure. This technique is very useful in event based application such as environment disaster monitoring, where event region changes very frequently and if we use structure based approach then we have to maintain the structure again and again. In structure free technique because we do not maintain any structure we don't have to reconstruct the structure at the time of node failure or the changing of event region. Mainly there are two main challenges in performing structure free data aggregation. First, as there is no pre constructed structure, routing decisions for the efficient aggregation of packets need to be made on-the-fly. Second, as nodes do not explicitly know their upstream nodes, they cannot explicitly wait on data from any particular node before forwarding their own data. The benefit of this approach is that we don't have to maintain the structure all the time whereas in structured environment we have to reconstruct the structure at the time of when some nodes fail due to energy failure [5]. Figure 8 shows Structure free Data Aggregation.

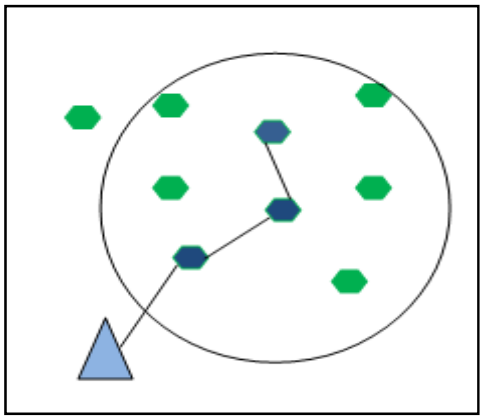

Figure.8 Structure free data aggregation

IV. ROUTING IN WIRELESS SENSOR NETWORK

In WSN, the sensor nodes have a limited transmission range, and their processing and storage capabilities as well as their energy resources are also limited. The design of routing protocols for WSNs is challenging because of several network constraints for example, energy, bandwidth, central processing unit, and storage. Routing in wireless sensor networks differs from conventional routing in fixed networks

in various ways. There is no infrastructure, wireless links are unreliable, sensor nodes may fail, and routing protocols have to meet strict energy saving requirements. Routing protocols for wireless sensor networks are responsible for maintaining the routes in the network and have to ensure reliable multi-hop communication. Data aggregation is one of the characteristic of the protocol, which is shown in Table I.

Table I. WSN Protocol Overview [9]

	SPIN	Directed Diffusion	Rumor Routing	LEACH	TEEN & APTEEN	GAF	GEAR	SAR	RMR
Classification	Flat	Flat	Flat	Hierarchical	Hierarchical	Location	Location	QoS	Flat
Mobility	Possible	Limited	Limited	Fixed BS	Fixed BS	Limited	Limited	No	Limited
Power Usage	Limited	Limited	N/A	Maximum	Maximum	Limited	Limited	N/A	Maximum
Negotiation Based	Yes	Yes	No	No	No	No	No	Yes	No
Data Aggregation	Yes	Yes	Yes	Yes	Yes	No	No	Yes	No
Localization	No	Yes	No	Yes	Yes	No	No	No	No
QoS	No	No	No	No	No	No	No	Yes	No
Scalability	Limited	Limited	Good	Good	Good	Good	Limited	Limited	Good
Multipath	Yes	Yes	No	No	No	No	No	No	No
Query Based	Yes	Yes	Yes	No	No	No	No	Yes	No

V. IMPACT OF DATA AGGREGATION IN WSN

There are two main factors that affect the performance of data aggregation methods in wireless sensor network, Such as energy saving and delay. Data aggregation is the process, in which aggregating the data packet coming from the different sources; – eliminating redundancy, minimizing the number of transmissions and thus saving energy. Delay is the latency connected with aggregation data from closer sources may have to held back at intermediate nodes in order to combine them with data from source that are farther away.

VI. CONCLUSION

Wireless sensors networks are an important type of resource-constrained distributed event-based system. In this Paper, We have presented survey of Data Aggregation techniques in wireless sensor networks. Data Aggregation can result in significant energy saving for a wide range of operational scenarios. We introduce the classification of data aggregation based on the network topology. Then we present the comprehensive study individual Data Aggregation technique. All of them focus on optimizing significant performance measures such as energy consumption, data latency, data accuracy, and network lifetime. Efficient formation, routing, and data-aggregation are the three most important focus areas of data-aggregation techniques. We have also outlined the main features of various data aggregation technique. Most of the existing work has primarily focused on the development of an efficient routing mechanism for data aggregation. However, the performance of the data-aggregation protocol is strongly united with the infrastructure of the network. Although, many of the data-aggregation techniques discussed look promising. At the end we mentioned factors affecting the Data Aggregation algorithms and Data Aggregation is the one of the characteristic of Routing Protocol.

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Use of Electronic Design Automation Tools for Communication Applications

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Abstract - In the present paper, the functionality of Binary Phase Shift Key (BPSK) transmitter is analyzed by using Xilinx, MATLAB-Simulink, Tanner and Cadence electronic design automation tools. The analyses determine the delay and power dissipation in the circuit. It can also be useful in pre-FPGA implementation of the circuit. The results show the versatility of various electronic design automation tools in communication engineering applications.

Keyword: *BPSK, Simulink, Xilinx, Tanner, Cadence.*

I. INTRODUCTION

In communication, modulation is the basic step for transmitting signals [1]. Depending on the type of signals, various modulation schemes are used. Binary Phase Shift Key (BPSK) is a modulation scheme in which phase of the carrier signal changes by 180^{o} with every change in polarity of information signal bits [2-3].

In the present work, BPSK transmitter is implemented using Xilinx, MATLAB-Simulink, Tanner and Cadence electronic design automation (EDA) tools. Through simulations, the functionality of BPSK transmitter is verified at various levels of abstraction. Xilinx works at gate-level [4-7], Matlab-Simulink works at block-level while Tanner and Cadence works at circuit level [8]. There is always a trade-off between accuracy and computation requirements at different abstractions levels.

The rest of the paper is arranged as follows. Section 2 gives a brief overview of BPSK scheme. Section 3 shows BPSK implementation using Xilinx and virtex-4 [9]. Section 4 gives implementation of BPSK using MATLAB Simulink. In section 5 Tanner EDA tool is used for implementation of BPSK transmitter. In section 6, it is implemented using Cadence. Section 7 contains simulations and results. Finally, conclusions are drawn in section 8.

II. BINARY PHASE SHIFT KEY MODULATION SCHEME

Modulation is the process in which some characteristic parameters of the high frequency carrier signal is varied according to the message or information signal. There are two types of communication systems viz. analog and digital. In analog communication, amplitude, frequency or phase modulation is used while in digital communication, depending on the presence of carrier signal these can be classified as base band or band bass data modulation schemes. BPSK modulation comes under band pass modulation scheme in which message signal is digital and analog carrier signal is used. The classification of various modulation schemes is shown in Fig. 1.

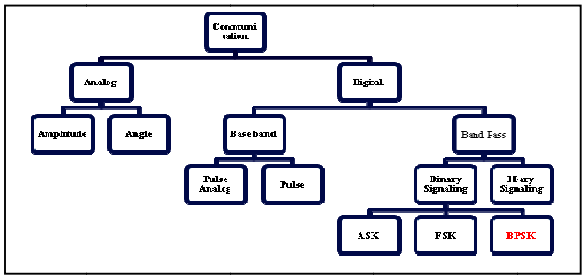

Fig.1 Classification of modulation schemes.

BPSK is sometimes also called as phase reversal keying (PRK). In BPSK, binary symbol '0' and '1' modulate the phase of the carrier signal. With every change in input signal bit, the phase of the carrier changes by 180^0. BPSK modulates only 1 bit/symbol at a time, hence it is useful for low data rate applications. The waveforms of BPSK modulation is shown in Fig. 2.

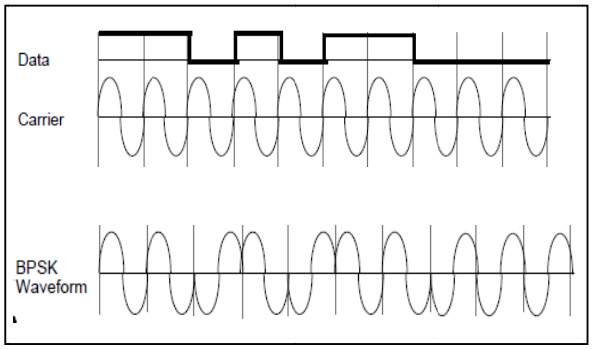

Fig.2 Waveforms of BPSK modulation

Owing to its simplicity BPSK is appropriate for low-cost passive transmitters and is used in vast number of applications. It is used in RFID standards such as ISO/IEC 14443 which has been adopted for biometric passports, credit cards such as American Express's ExpressPay. It is used in IEEE 802.15.4 (zigbee) standards. Phase modulations are also used in space and satellite communication.

III. BPSK IMPLEMENTATION USING XILINX AND VIRTEX-4

Xilinx consists of hardware description language (HDL) such as Verilog and VHDL. The hardware description languages describe the architecture and behavior of integrated and discrete electronic systems. In the present work Verilog is used for simulative analysis. Verilog had been started initially as a hardware modeling language by Gateway Design Automation Inc. around 1984. It permits designer to design the system using bottom-up or top-down methodology.

The various modules used for implementation of Binary Phase Shift Key modulation scheme are pseudo random (PR) bit generator, polar conversion sine generator, multiplier and input section. Fig. 3 depicts the block diagram representation of BPSK scheme.

Verilog works at gate level of abstraction. Each individual block is synthesized using bottom-up approach.

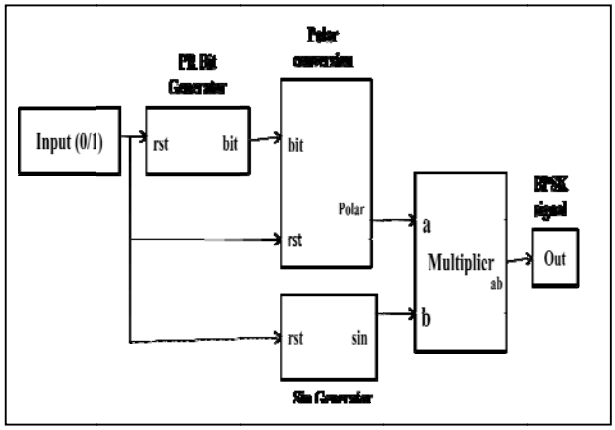

Fig.3 Block diagram of BPSK transmitter in Xilinx

The pseudo random bit generator is used to form the message signal bits according to input bit. The sine generator generates the sine waveform. It is converted into five bits where most significant bit shows the polarity of the sine wave. The sin generator is synthesized using test bench. The output of PR bit generator and sine wave generator is given to the input of multiplier. The output of multiplier is a BPSK signal.

IV. BPSK IMPLEMENTATION USING MATLAB-SIMULINK

MATLAB is a commercial "Matrix Laboratory" package which operates as an interactive programming environment. It is a high-level language that enables designers to perform computationally intensive tasks such as numerical computations, display information graphically in 2D and 3D and helpful in solving many engineering and science application problems. It contains an additional package namely Simulink that adds graphical multi-domain simulation and model-based design for dynamic and embedded systems. It includes an extensive block library of toolbox for both linear and nonlinear analyses. Models are hierarchical, which allows both top-down and bottom-up approaches.

In the present case, Simulink is used for implementation of BPSK modulation. Simulink works at block level of abstraction. It uses PN sequence generator, unipolar to bipolar converter, sine wave generator and multiplier for its operation. Scope represents the display unit on which output waveforms can be analyzed. The block diagram is shown in Fig. 4.

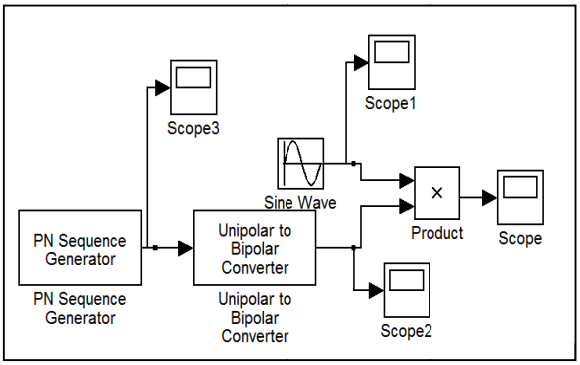

Fig.4 Block diagram of BPSK transmitter in Simulink.

In Fig.4, PN sequence generator produces pseudo random bits as input. Its voltage swing varies between 0 and 1. It is then given to unipolar to bipolar converter. This converts unipolar signal to bipolar i.e. its polarity varies between -1 and 1. The sine wave generator produces sine signal. Both the inputs are given to the multiplier which gives BPSK siganal at its output. It is analyzed using scope.

V. BPSK IMPLEMENTATION USING TANNER EDA TOOL

Tanner EDA tool is a complete software suite for the design, layout and verification of analog, mixed-signal, RF and MEMS ICs. It enables designers to work on both front end and back end platforms.

Various analyses such as schematic capture, circuit simulation and waveform probing to physical layout and verification can be performed using this tool. It includes S-Edit for schematic capture, T-Spice for circuit simulation and W-Edit for waveform viewing and analysis.

BPSK is implemented using Tanner EDA tool and analysis is carried out at circuit-level of abstraction.

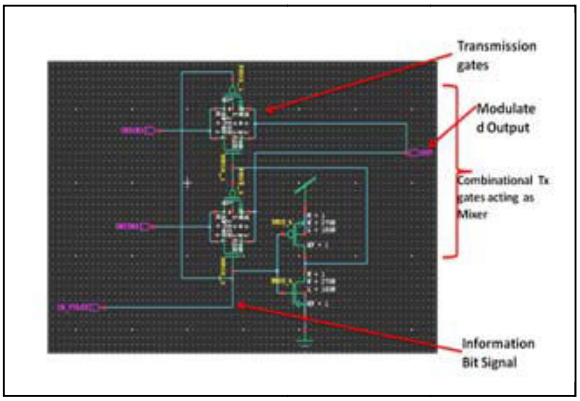

Fig.5 Block diagram of BPSK transmitter in Tanner EDA tool.

Working at circuit level gives more accuracy as designers have flexibility of defining device parameters. At circuit level various process variations can be carried out so as to get optimum results. The schematic of BPSK transmitter using Tanner EDA tool is shown in Fig. 5.

The schematic shown in Fig.5 is drawn in S-Edit. The signal information bit is given through pulse signal. The mixer is drawn using combination of transmissions gates. The transmission gates give lesser delay and hence it gives faster response.

VI. BPSK IMPLEMENTATION USING CADENCE

Cadence is the most widely used and preferred EDA tool design solution in VLSI and semiconductor industry. It allows and supports all the stages of IC design and verification. It consists of schematic design editor, virtuoso: Layout design editor, Spectre, Analog Artist which consists of integrated simulation environment and many more. The BPSK is implemented using Cadence and is shown in Fig. 6.

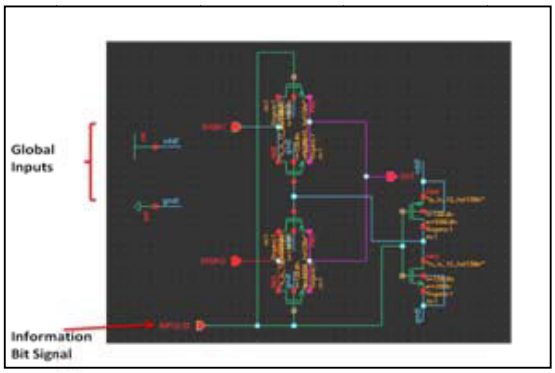

Fig.6 Block diagram of BPSK transmitter in Cadence.

VII. RESULTS AND DISCUSSION

The BPSK is simulated using Xilinx-Verilog HDL. The RTL schematic of the BPSK transmitter is shown in Fig. 7. It shows gate level representation of the circuit.

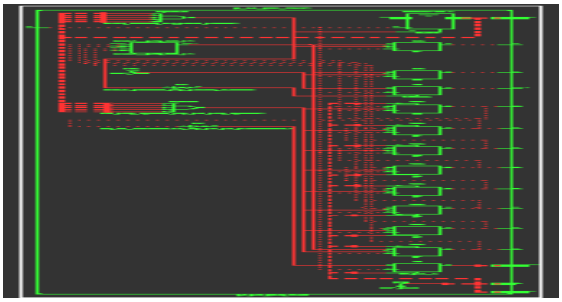

Fig.7 RTL schematic of BPSK transmitter.

The output waveforms are shown in Fig.8. It is seen that MSB of modulated waveform changes its polarity as the information changes from 1 to 0.

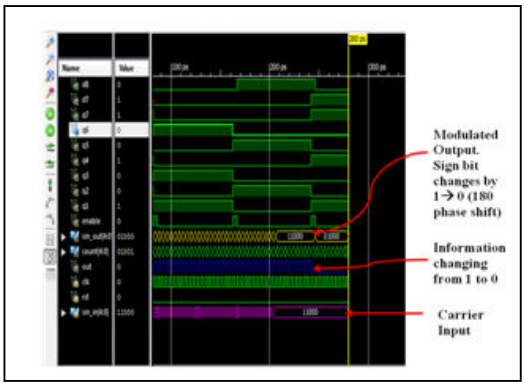

Fig.8 Waveforms of BPSK transmitter in Xilinx.

The on-chip power dissipation with respect to temperature in BPSK is calculated using Xilinx Virtex-4. It is seen that power dissipation increases with temperature. With rise in on chip power heat dissipation in the device will increase and the device may burn out. Hence this gives operating range/ safe range of a device over which it will show favorable results. The on-chip power variation with temperature is as seen in Fig. 9. For example, for temperature varying from 25^0 C to 100^0 C, the percentage variation in power is 64.179%.

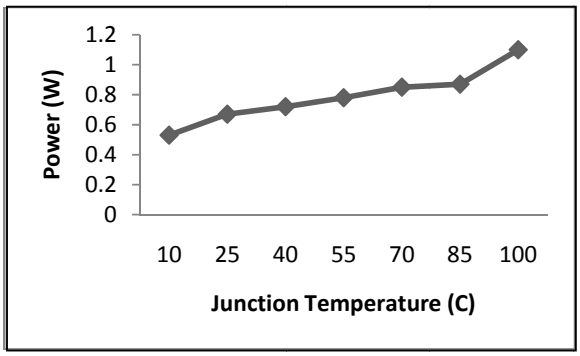

Fig.9 On-chip power variation with temperature.

Fig. 10 gives on-chip power variation with different signal function. The power dissipation due to leakage current dominates amongst all sub modules namely leakage, clock, logic, I/O, SRAM, DCM, PLL and DSP as seen in Fig.10. Consequently, it is always a challenge to design optimal circuits so as to have minimum delay and power dissipation in the circuit.

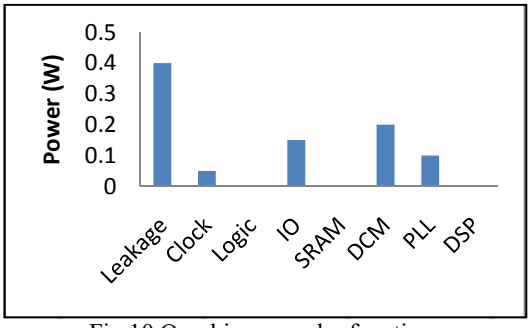

Fig.10 On-chip power by function.

Furthermore, BPSK modulation is implemented using MATLAB-Simulink. The waveforms are shown in Fig.11.

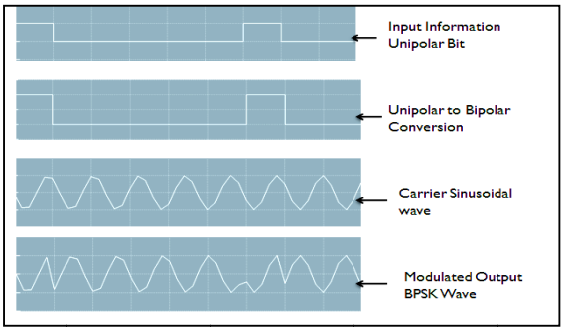

Fig.11 Waveforms of BPSK transmitter using MATLAB- Simulink

It can be seen that phase of the modulated output changes by 180^0 with every change in information bit.Fig. 12 shows implementation of BPSK transmitter using Tanner EDA tool. The transient analysis is carried out. The carrier frequency of the BPSK transmitter is taken as 50 MHz. Delay and power dissipation in the circuit is calculated using Spice. The delay is found to be 3.2855ns and power dissipation in the circuit is 4.589watt. The waveforms are seen in W-Edit. It can be analyzed from Fig.12 that modulated output changes by 180^o with change in information bit signal.

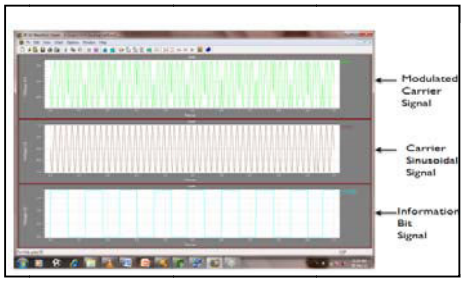

Fig.12 Waveforms of BPSK transmitter using Tanner.

The modulated, carrier signal and information signal waveforms are seen in Fig. 13. Here Cadence is used for implementation of BPSK Transmitter.

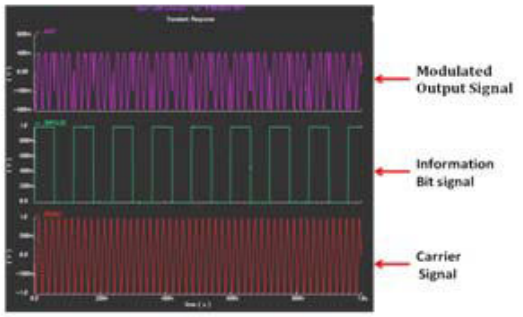

Fig.13 Waveforms of BPSK transmitter using Cadence

VIII. CONCLUSIONS

In the present analyses, the BPSK modulation is carried out using different EDA tools. Modulation and simulations are carried. Analysis is carried out at different abstraction levels. Effective analysis gives optimum desired results.

Using Xilinx, RTL schematic is obtained. Also, on-chip power dissipation and variation of on-chip power with temperature are analyzed using Xilinx Virtex-4. In MATLAB, block level implementation of BPSK is done and its inputs and output waveforms are analyzed. Further, BPSK transmitter is implemented at circuit level using Tanner and Cadence EDA tools. Mixer of the BPSK transmitter is implemented using transmission gates which are generally useful for faster circuit response. Also, delay and power analysis is carried out.

The analyses show the versatility of EDA tools. Depending on the accuracy, time requirement and working environment different EDA tools can be used. These tools can be used in various electronics and communication engineering applications and are helpful in providing solutions for various scientific problems.

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